Airbus Crisa

RISC-V Soft Core Processor for Space Microcontroller Applications

40 ANNIVERSARY Airbus Crisa

CRISA

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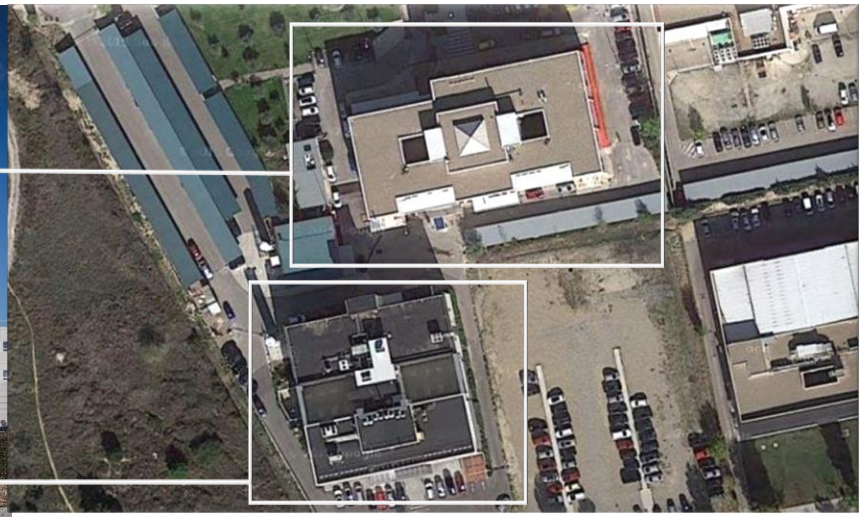
RISC-V In Space Workshop, 2-3 April 2025, Gothenburg, Sweden

AIRBUS

Airbus Crisa Facilities in Tres Cantos

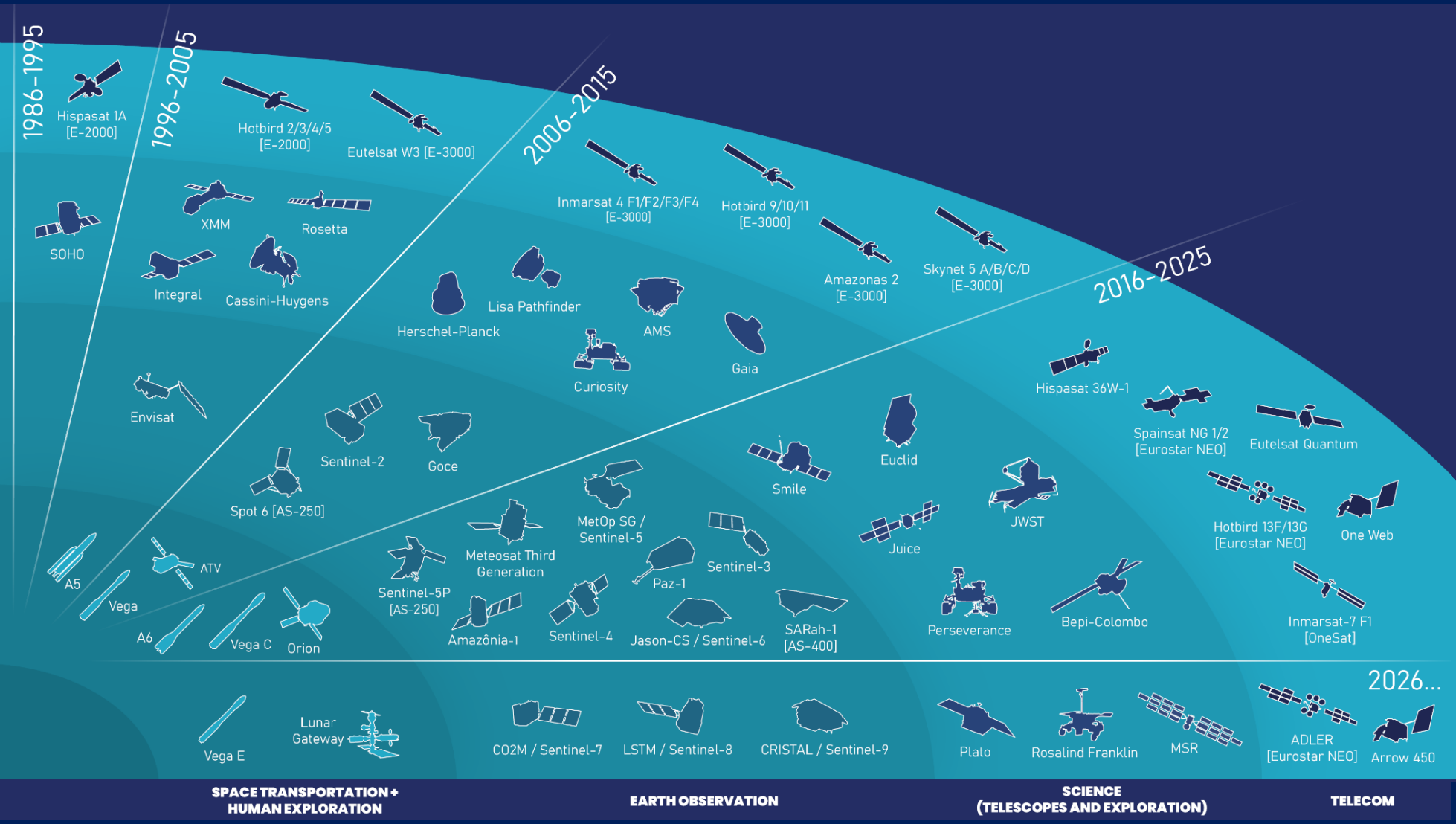


95 M€ Sales

500+ employees

107 M€ Contracted

Flagship Missions



TELECOM
PLATFORMS

Eurostar 2000, Eurostar 3000 and Eurostar NEO

>100 SATELLITES LAUNCHED.

EARTH OBSERVATION
PLATFORMS

AstroSat 250

19 SATELLITES LAUNCHED

LAUNCHERS

ARIANE 5, ARIANE 6, VEGA, VEGA C

> 135 LAUNCHES

300 + accomplished missions

2000 + flight units launched

8.700 + kg launched

75 missions in progress

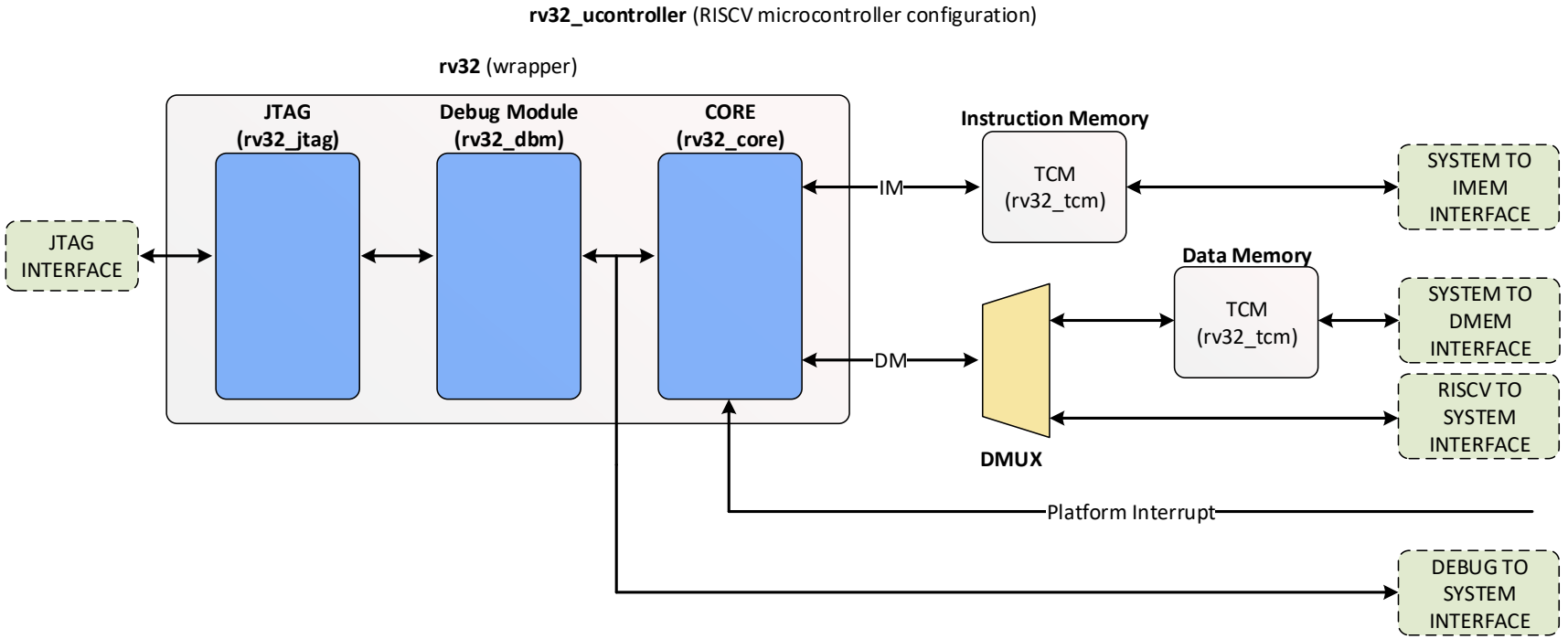
AIRBUS

RISC-V Soft Core Processor: Overview

- RISC-V Core Features
  - Harvard architecture
  - 32-bit data / address space
  - RV32I, M and F extensions
  - Implementation SEU protected
  - Interrupts:
    - 16 interrupt sources / 6 exceptions
    - Traps jump to the same base address
    - Nested traps are not supported
  - Tightly Coupled Memory (instruction/data)
    - Hamming code for SEC and DED
    - Programmable autonomous scrubbing
- Software
  - C programming (Linux / Windows)
  - Both open-source / proprietary IDE
- Debug Module with JTAG connection
  - SW Debugging on HW platform via JTAG
  - Linux (Ubuntu 22.04 LTS) / Windows 10
- Embedded microcontroller applications in FPGAs
  - Small ICUs / low / mid range processing power
  - Replacement proprietary solutions (expensive / fixed)
- Modular and flexible implementation
  - Minimize resources / Maximize performances

RISC-V Soft Core Processor: Architecture, *rv32* and *rv32_ucontroller*

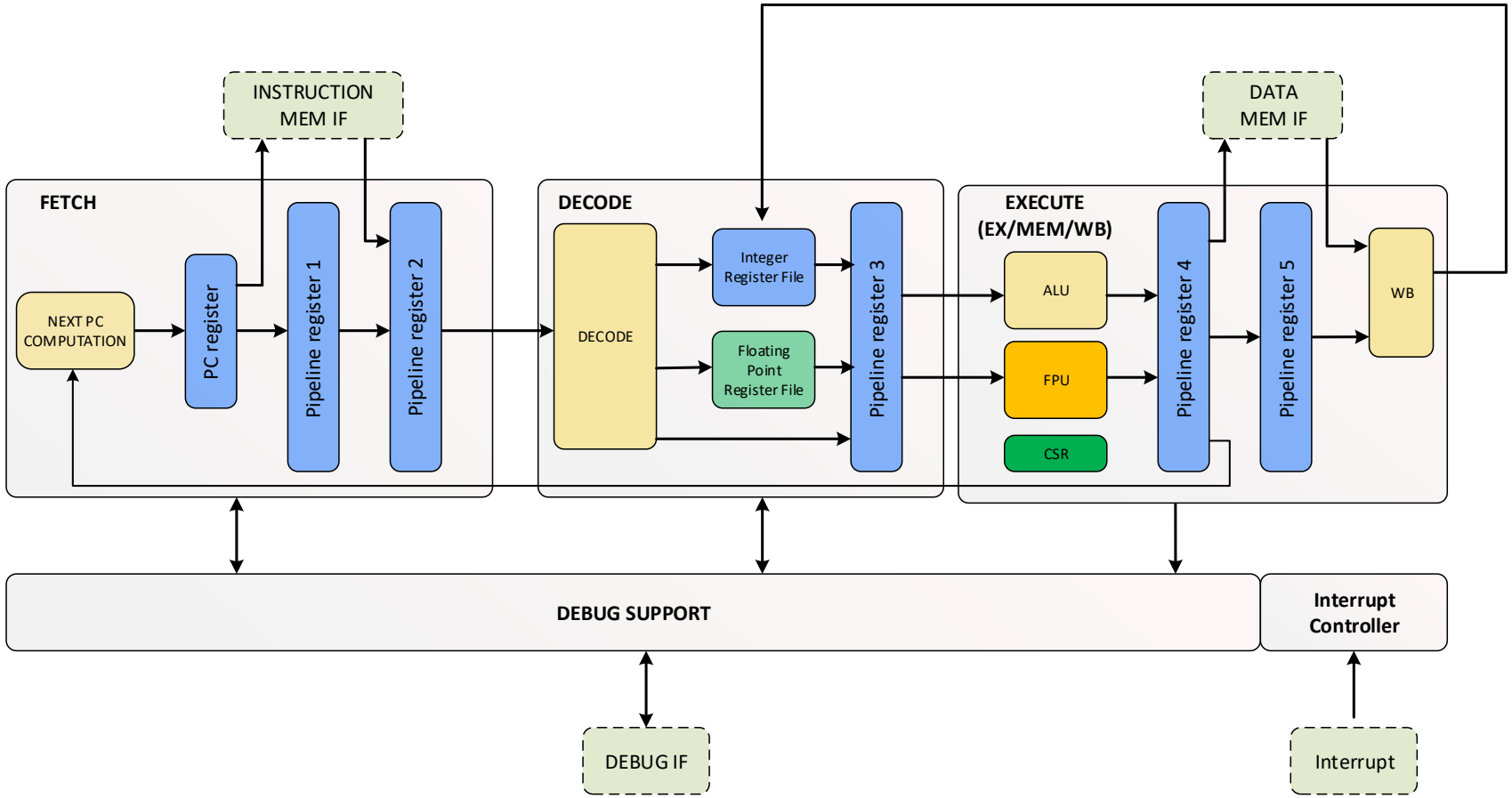
- ***rv32*** is the main module.
  - You can use this module
  - But better use configurations:
    - ***rv32_ucontroller***
    - ***rv32_uprocessor***
- ***rv32*** a wrapper of three sub-modules
  - ***rv32_jtag***: JTAG module
  - ***rv32_dbm***: Debug module
  - ***rv32_core***: RISC-V core
    - implements the RISC-V ISA supported extensions (I, M, F)



- ***rv32_ucontroller*** is a configuration module
- ***rv32_tcm***: TCM module, hamming protected (SEC, DED), scrubbing, for imem and dmem
- ***rv32_tcm***: TCM IF to *rv32_core,* and generic backend IF for bus connection (no burst support) (APB, AXI lite…)

RISC-V Soft Core Processor: *rv32_core* Pipeline

- 6 stage pipeline
- Built for internal FPGA memory
- Tightly coupled memory pipeline interface
- One instruction per clock cycle
  - Cycle N: Addr / Inst(Addr-4)
  - Cycle N+1: Addr+4 / Inst(Addr)
- Cache support
  - Already built in the pipeline, for instruction and data memory
- Memory scrubbing support
  - Already built in the pipeline, for instruction and data memory



RISC-V Soft Core Processor: Performances

- FPGA resources and frequencies

RISC-V Configuration	LUT	FF	BRAM	DSP	Est. Freq (syn.)	Device
RV32I ext 64KB imem/64kB dmem (+EDAC)	7236	2861	128	0	70MHz	Commercial
RV32IMF ext 64kB imem/64kB dmem (+EDAC)	21389	4445	128	8	> 40MHz	Commercial
RV32I ext 64KB imem/64kB dmem (+EDAC)	8373	3452	128	0	50MHz	RT4G150
RV32IMF ext 64KB imem/64kB dmem (+EDAC)	20996	5043	128	8	> 30MHz	RTG4150

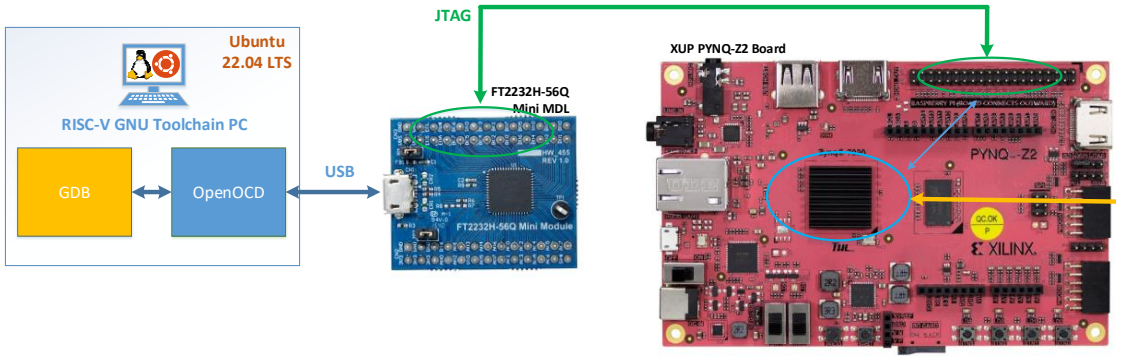
- Standard Benchmarks in HW platform

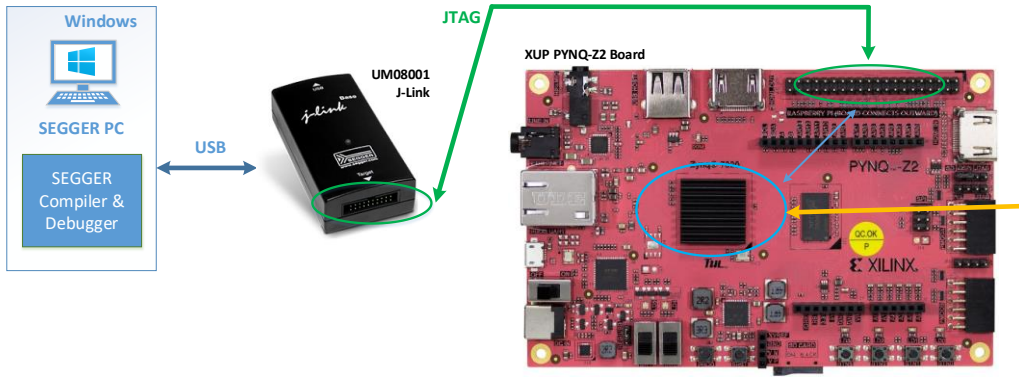
Configuration	Dhrystone in HW (@48MHz)	Coremark in HW (@48MHz)
GCC compiler O2 optimization No inlining Standard libraries RV32I (only I ext, no M ext)	65932 Dhrystones/s 37.5 DMIPs 0.78 DMIPs/MHz	40 Iterations/s 0.83 Coremark/MHz

RISC-V Soft Core Processor: SW Development Environment

- Open Source RISC-V GNU Toolchain
- Linux (Ubuntu 22.04 LTS)
  - GNU gcc compiler
  - GDB debugger
  - Support OpenOCD
  - FT2232H-56Q Mini MDL USB to JTAG connection

- SEGGER IDE
- Windows 10.
  - Proprietary C compiler and debugger
  - Support for GNU gcc compiler
  - J-Link UM08001 HW adapter, USB to JTAG





RISC-V Soft Core Processor: Verification

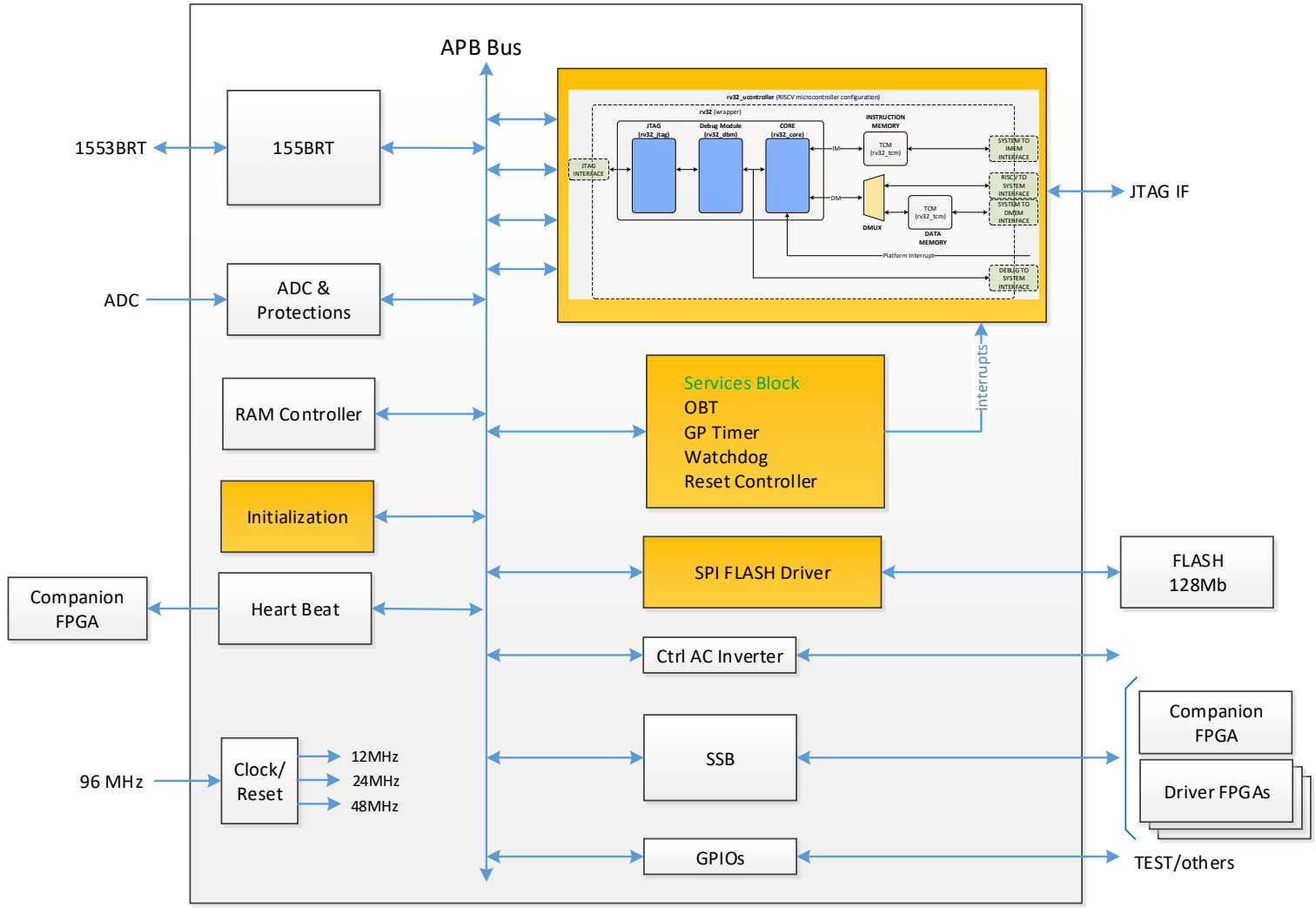
- ECSS FPGA design flow
- Simulations based on OSVVM
  - functional coverage, and constrained random tests
  - allows SW-VHDL integration tests by doing co-simulation
- Module verification done at different levels:
  - **Unitary simulations** have been done on the following modules
    - *rv32_core*, *rv32_jtag*, *rv32_dbm*, *rv32_tcm*
  - **Integration simulations** have been done on the following modules
    - *rv32_ucontroller*
  - **Hardware Tests** have been done on the following levels
    - Debugging chain: OpenOCD + *rv32_jtag* + *rv32_dbm* + *rv32_core*
    - Comparison tests *rv32* vs NEORV32 soft core processor (I and M ext)
- Type of tests:
  - RISC-V Architecture Compatibility Tests passed for I, M and F (sims)
  - Directed tests, Stress tests, Constrained Random tests passed (sims)

Unitary Test sequences	Result	Remarks
test000000_rv32_core_official_ext_i	Passed	Official ACT tests
test000001_rv32_core_official_ext_m	Passed	Official ACT tests
test000010_rv32_core_corner_ext_i	Passed	Corner tests
test000011_rv32_core_corner_ext_m	Passed	Corner tests
test000020_rv32_core_sdext_ext_i	Passed	Debug tests
test000021_rv32_core_sdext_ext_m	Passed	Debug tests
test000030_rv32_core_benchmarks_ext_i	Passed	
test000031_rv32_core_benchmarks_ext_m	Passed	
test000401_crip_rv32_tcm_unit_scb	Passed	
test000400_crip_rv32_tcm_unit_basic	Passed	
test000402_crip_rv32_tcm_unit_scb_error	Passed	
test000403_crip_rv32_tcm_unit_mem_if	Passed	
test000404_crip_rv32_tcm_unit_corner	Passed	
test000405_crip_rv32_tcm_unit_auto_init	Passed	
test000406_crip_rv32_tcm_unit_bus_size	Passed	
test000407_crip_rv32_tcm_unit_unprotected	Passed	
test000300_rv32_jtag_behaviour	Passed	
test000900_rv32_sim_core_official_ext_i	Passed	Official ACT tests
test000901_rv32_sim_core_official_ext_m	Passed	Official ACT tests
test000910_rv32_sim_core_corner_ext_i	Passed	Corner tests
test000911_rv32_sim_core_corner_ext_m	Passed	Corner tests
test000920_rv32_sim_core_sdext_ext_i	Passed	Debug tests
test000921_rv32_sim_core_sdext_ext_m	Passed	Debug tests
test000930_rv32_sim_core_benchmarks_ext_i	Passed	
test000931_rv32_sim_core_benchmarks_ext_m	Passed	
test000600_rv32_core_combination_ext_i	Passed	Combination of 3 instr
test000601_rv32_core_combination_ext_m	Passed	Combination of 3 instr
test000610_rv32_core_rand_arith_ext_i	Passed	Random
test000611_rv32_core_rand_arith_ext_m	Passed	Random
test000620_rv32_core_rand_mem_ext_i	Passed	Random
test000621_rv32_core_rand_mem_ext_m	Passed	Random
test000630_rv32_core_rand_branch_ext_i	Passed	Random
test000631_rv32_core_rand_branch_ext_m	Passed	Random
test000100_rv32_dbm_cntrl_registers	Passed	
test000101_rv32_dbm_cntrl_states	Passed	
test000102_rv32_dbm_proc_mem	Passed	
test000103_rv32_dbm_proc_reg	Passed	

A subset of the test cases for I and M ext

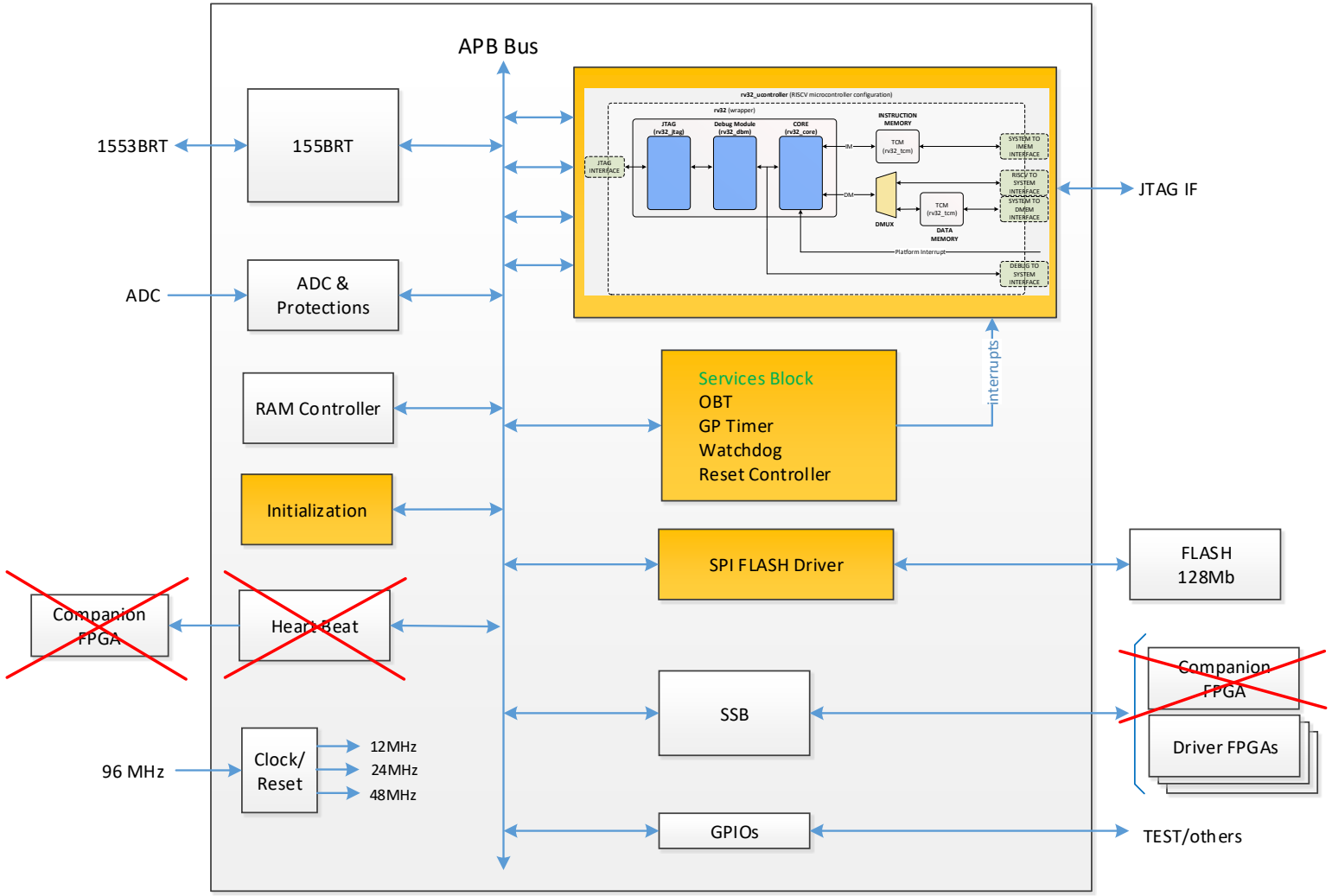
RISC-V Soft Core Processor: Project #1 TMTC & Control (Petri diagrams)

- TMTC & Control (Petri diagrams)
- Mission time: Years
- *rv32_ucontroller*
- SW Stack
  - Drivers (Class A)
  - BareMetal Application (Class B)
- Monitoring Companion RadHard FPGA
  - Listen Heart Beat from RISC-V main FPGA
  - Re-initialize RISC-V main FPGA if no Heart Beat
- Initialization
  - No boot SW
  - VHDL loads Baremetal App, and params
  - Images EDAC and CRC protected in Flash (x3)
- Services Block
  - Collects interrupt sources
  - Watchdog, GP Timers, OBT
  - Reset controller



RISC-V Soft Core Processor: Project #2 TMTC & Motor Control

- TMTC & Control (State Diagrams)
- Mission time: Hours
- *rv32_ucontroller*
- SW Stack
  - Drivers (Class A)
  - Boot SW (Class A)
  - Application SW (Class A)
- ~~Monitoring Companion RH FPGA~~
- Initialization
  - VHDL loads the boot SW, and other params
  - VHDL gives control to boot SW after loading
  - Boot SW loads App SW and handles control
  - Images EDAC and CRC protected in Flash (x3)
- Services Block
  - Collects interrupt sources
  - Watchdog, GP Timers, OBT
  - Reset controller



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Thank you!