FRONTGRADE Gaisler

SEE Characterization of NOEL-V on 28nm FD-SOI Platform for Space

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Agenda

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01

Introduction

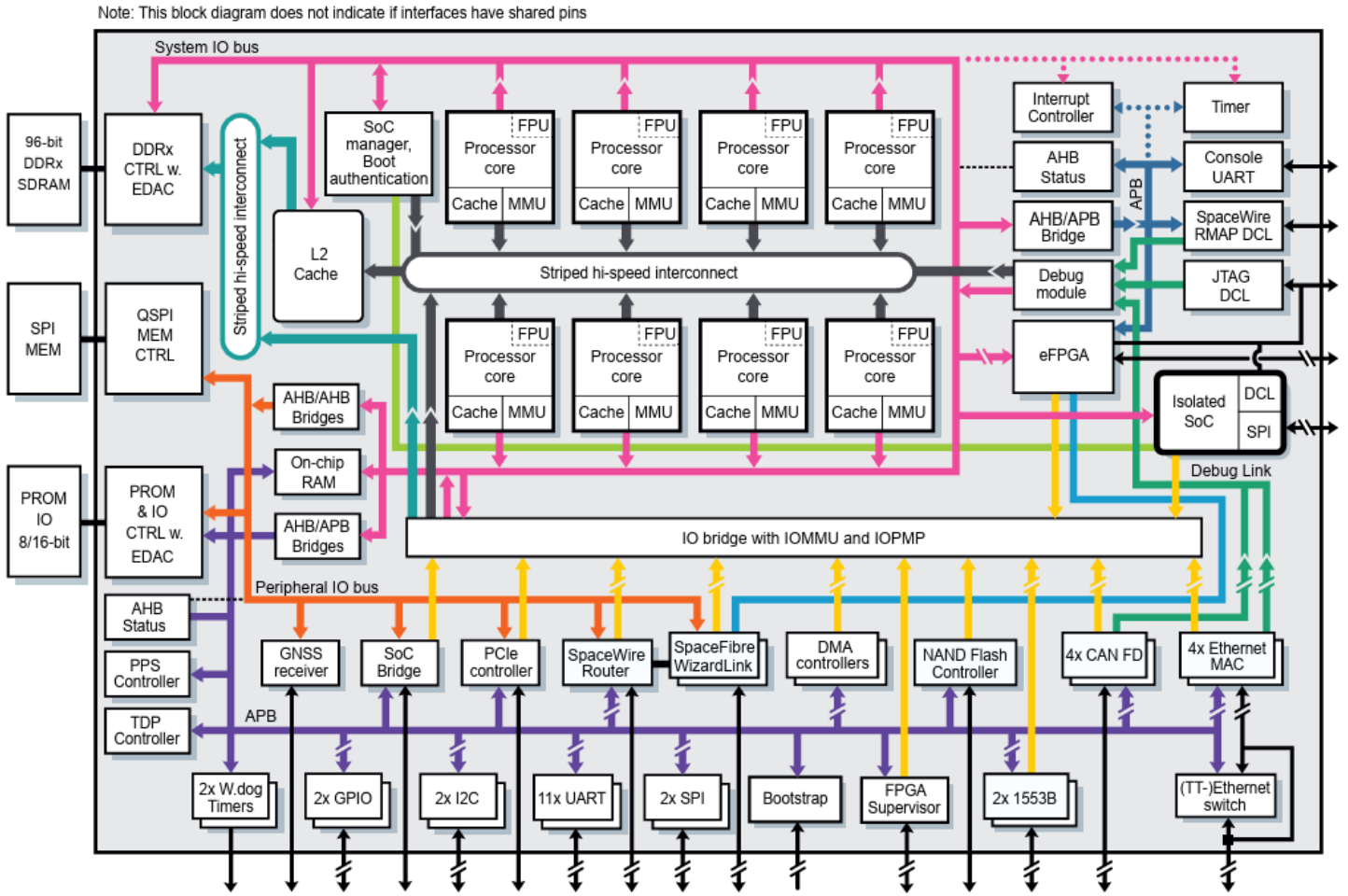
Introduction

Background / Motivation

- Frontgrade Gaisler's next generation space-grade processor
  - GR765 radiation-hardened fault-tolerant octa-core system-on-chip
    - Dual-ISA – RISC-V RV64GCH and SPARC V8
    - Based on STMicroelectronics' 28nm FD-SOI GEO P2 platform for Space

Objectives

- Evaluate the performance of the NOEL-V processor implemented on STM's 28nm FD-SOI platform for Space for Single Event Effects



Wednesday, April 2nd, 17:00
"GR765 – Octa-Core Rad-Hard Microprocessor," Magnus Hjorth – Frontgrade Gaisler

02

NOEL-V processor

NOEL-V processor

Characteristics

- RISC-V processor core
  - Highly configurable
  - 64- or 32-bit architecture
  - 7-stage in-order pipeline (dual- or single-issue)
    - Late ALUs, branch units, dynamic branch prediction
  - L1 caches
    - Separate Instruction and Data caches
    - Up to 4 ways, 16KB each
    - Write buffer, snooping for coherency
  - Fault tolerance features
    - Well-stablished features following the high standard of the LEON processor line
  - Leverages general RISC-V software and tool support together with our software ecosystem

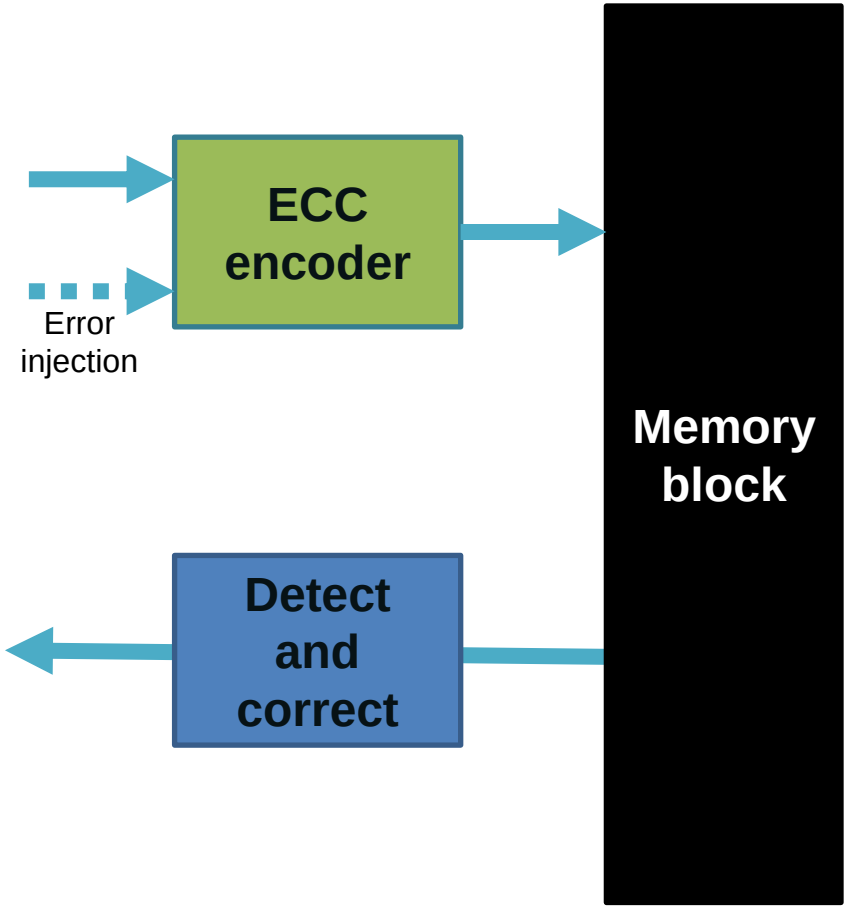
Additional information
Frontgrade Gaisler presentations
https://www.gaisler.com/noel-v

Primary feature set

- RISC-V RV64GCH or RV32GCH
  - Can run complex OS (like Linux), also within a virtual machine
- AHB and AXI4 bus support

NOEL-V processor – Fault tolerance overview

- Protection of memory blocks (register file and caches) using error correcting codes
  - Protected with a full SECDED code with custom patented scheme
    - Deliver correct data locally without causing memory access
    - Guaranteed detection also of 3-bit and 4-bit adjacent bit errors
- Hardware scrubber built into processor (register file and caches) to avoid error build-up
  - Removes need for manual scrubbing routines
- Error counters and diagnostic interfaces
  - Monitor and inject errors



NOEL-V processor – Custom L1 cache error correction scheme

- Each 32-bit word is protected by 8 checkbits
  - Correct 1-bit error and detect 2-bit error (similar to conventional 32+7 BCH protection)
  - Top half of the check bits (4 bits) is also the logical XOR of the other codeword nibbles
- Detect error by simple parity check (shorter critical paths - higher fmax)
- Guaranteed detection also of 3-bit and 4-bit adjacent bit errors
  - (Heavy ion-induced MBUs on some technologies)
- Corrections done transparently in cache controller, without involving software or bus
  - Invalidate cache line if uncorrectable (write-through)
- Built-in configurable scrubber, to avoid error build-up
- Counters for detected issues, diagnostic interface

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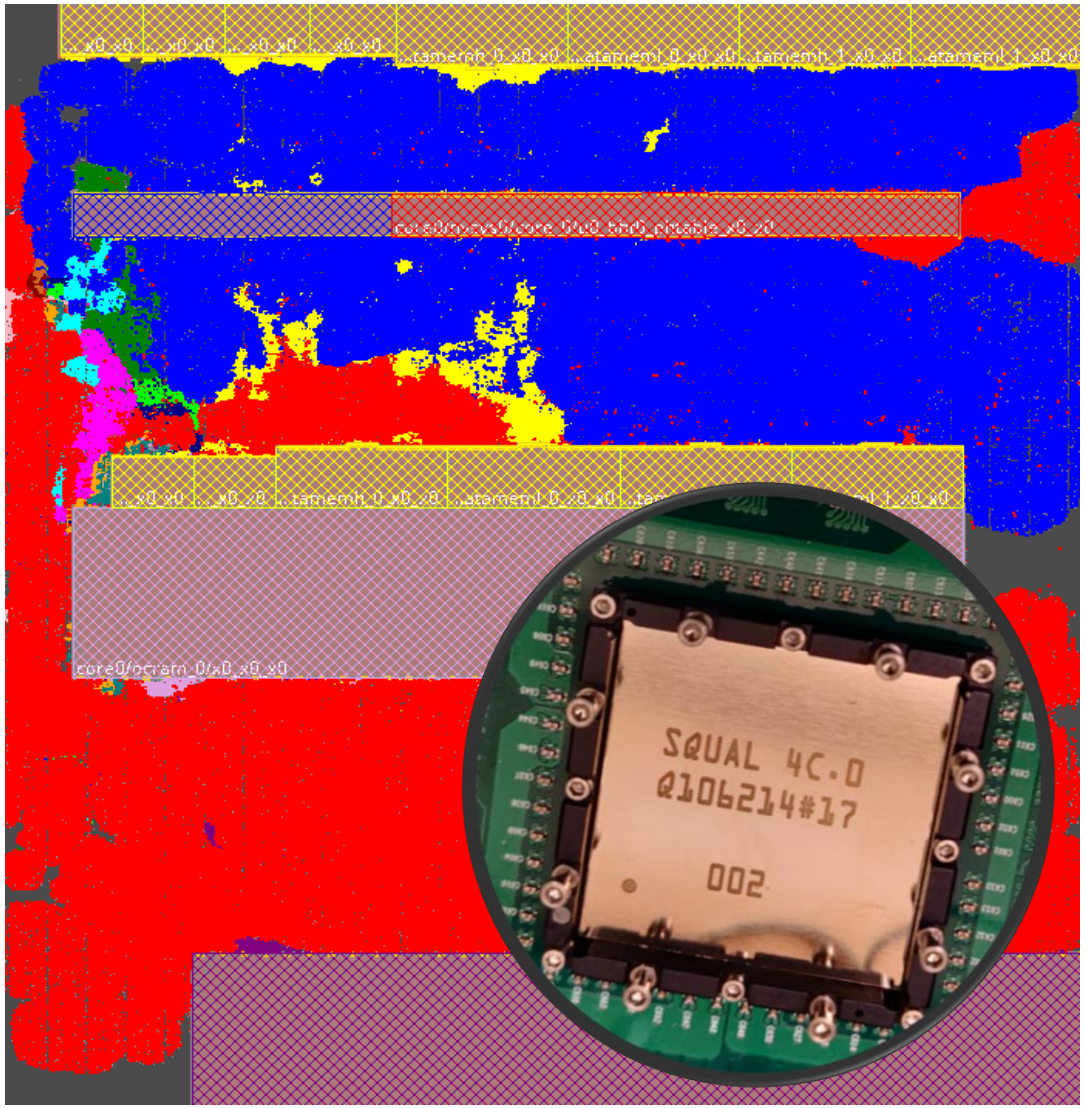
03

Device under test

Device under test

Radiation-hardened demonstrator with NOEL-V 64-bit RISC-V and LEON5 32-bit SPARC V8 processors

- STMicroelectronics' 28nm FD-SOI GEO P2 platform for Space
  - SEU – Radiation-hardened cells
  - SEL – Intrinsic SEL immunity in SOI areas
  - TID – Fully characterized up to 50 krad(Si)
  - Forward Body-Biasing (FBB) support
- Specialized design with NOEL-V and LEON5 sharing resources
- Proves implementation on the target technology
- Collaboration between STM and Gaisler R&D teams
- Manufactured using European supply chain



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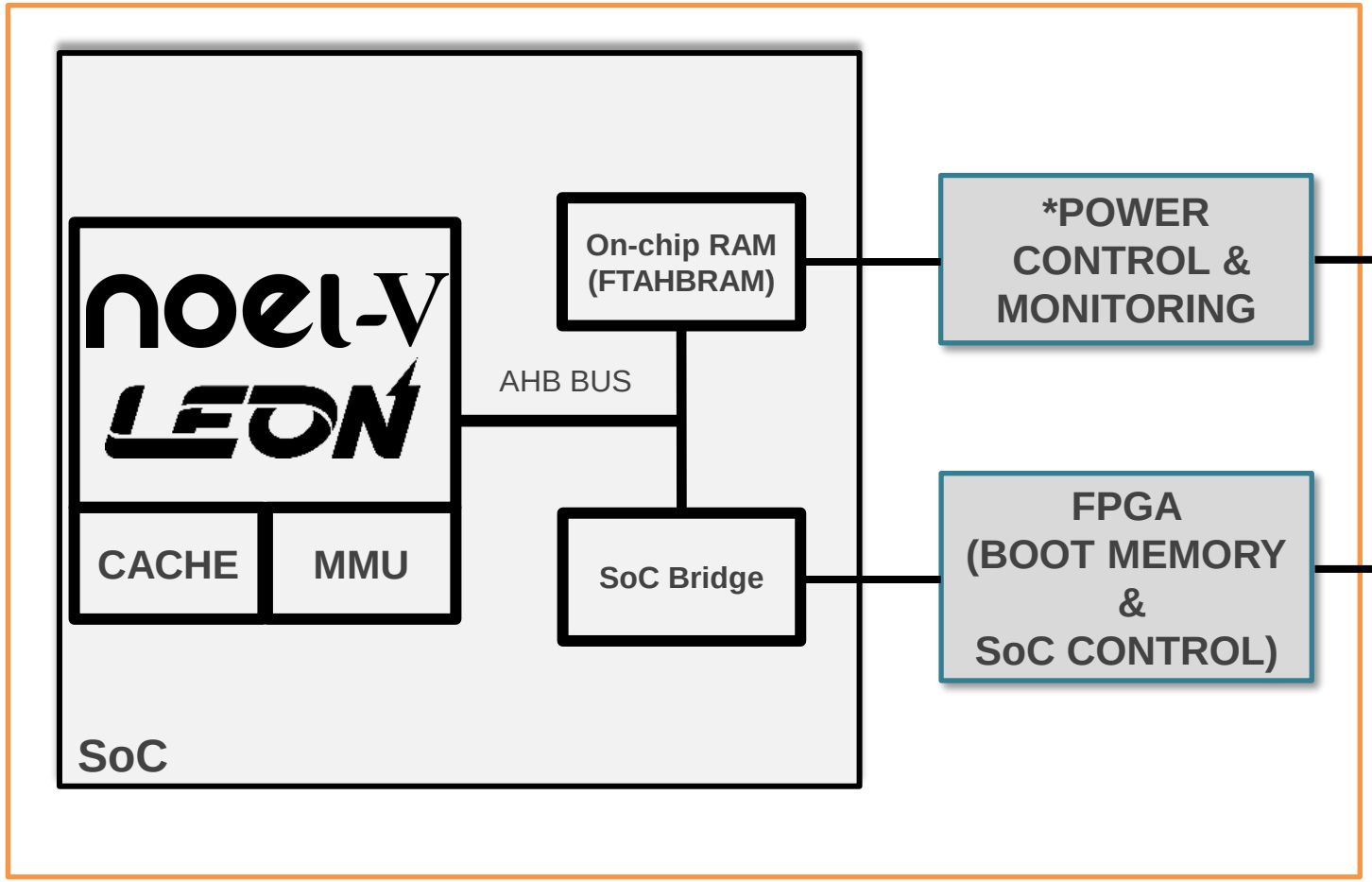
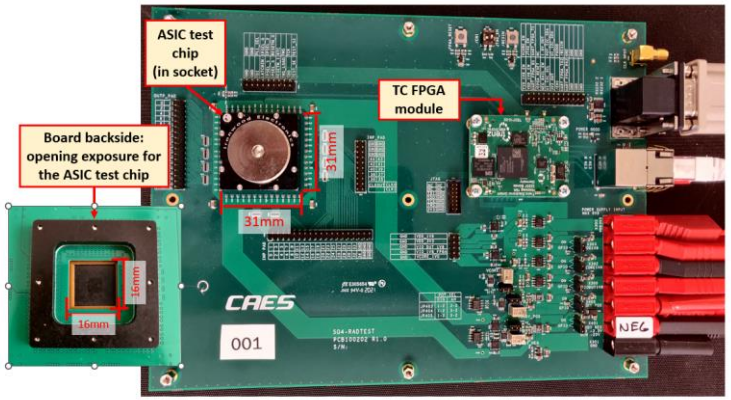
04

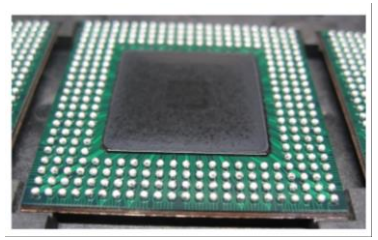
SEE characterization

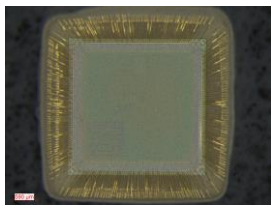
SEE characterization – Hardware

TEST BOARD









* SoC core voltage (VCORE) and body bias (VBODY) are configurable

SEE characterization – Software

Bare-metal test cases software

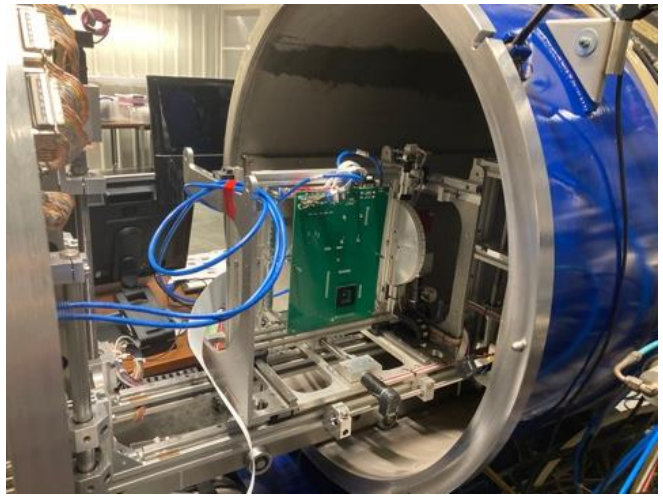
- Integer unit – To exercise the register file and L1 cache
- Paranoia – To exercise the floating-point unit
- Stanford – A set of benchmarks for general processor tests, such as sorting, FFT, puzzle, towers of Hanoi, permutation, and matrix multiplication

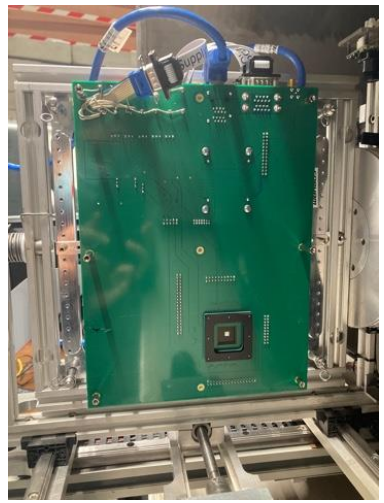
Monitoring

- Silent Data Corruption (SDC)
- Single Event Functional Interrupt (SEFI)
- Error counters
  - Detected and corrected errors in memory elements, such as register file, L1 cache, and FTAHBRAM
  - The software execution is not affected when a memory error is corrected

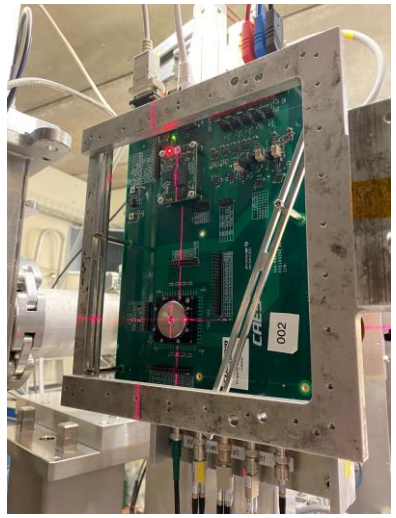
SEE characterization – Test campaigns

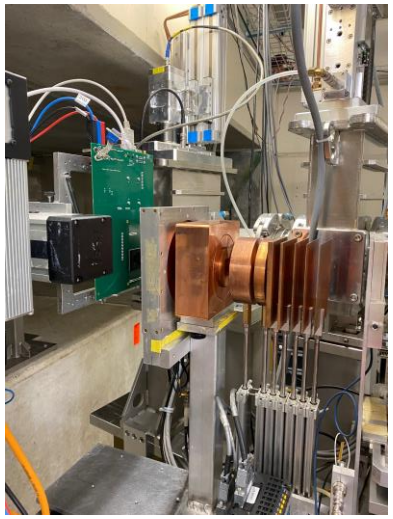
Heavy ions testing
- HIF/UCL, Belgium
- Full LET range, from 1.3 to 91.9 MeV·cm²/mg
- Flux from 7E+2 to 1.5E+4 p/cm²/s
- Fluence per run from 5E+5 to 5E+7 p/cm²
- 8 hours beam time





Protons testing
- PIF/PSI, Switzerland
- Energies of 23.5, 101.4, and 230 MeV
- Flux from 8E+7 to 1E+8 p/cm²/s
- Fluence per run from 2E+10 to 1E+11 p/cm²
- 12 hours beam time





05

SEE results

SEE results – Heavy ions

NOEL-V (NV) and LEON5 (L5) processors tested at different frequencies and bias conditions

Target	Frequency (MHz)	VCORE (mV)	VBODY* (mV)	Description
NV-HI	400	1100	1100	High frequency, maximum core voltage (1100 mV), and high-performance body bias (1100 mV)
NV-LF	250	670	1100	Low frequency, lowest core voltage (670 mV), and high-performance body bias (1100 mV)
L5-HI	500	1100	1100	High frequency, maximum core voltage (1100 mV), and high-performance body bias (1100 mV)
L5-GX	500	900	0	High frequency, low core voltage, low leakage body bias (0 V)

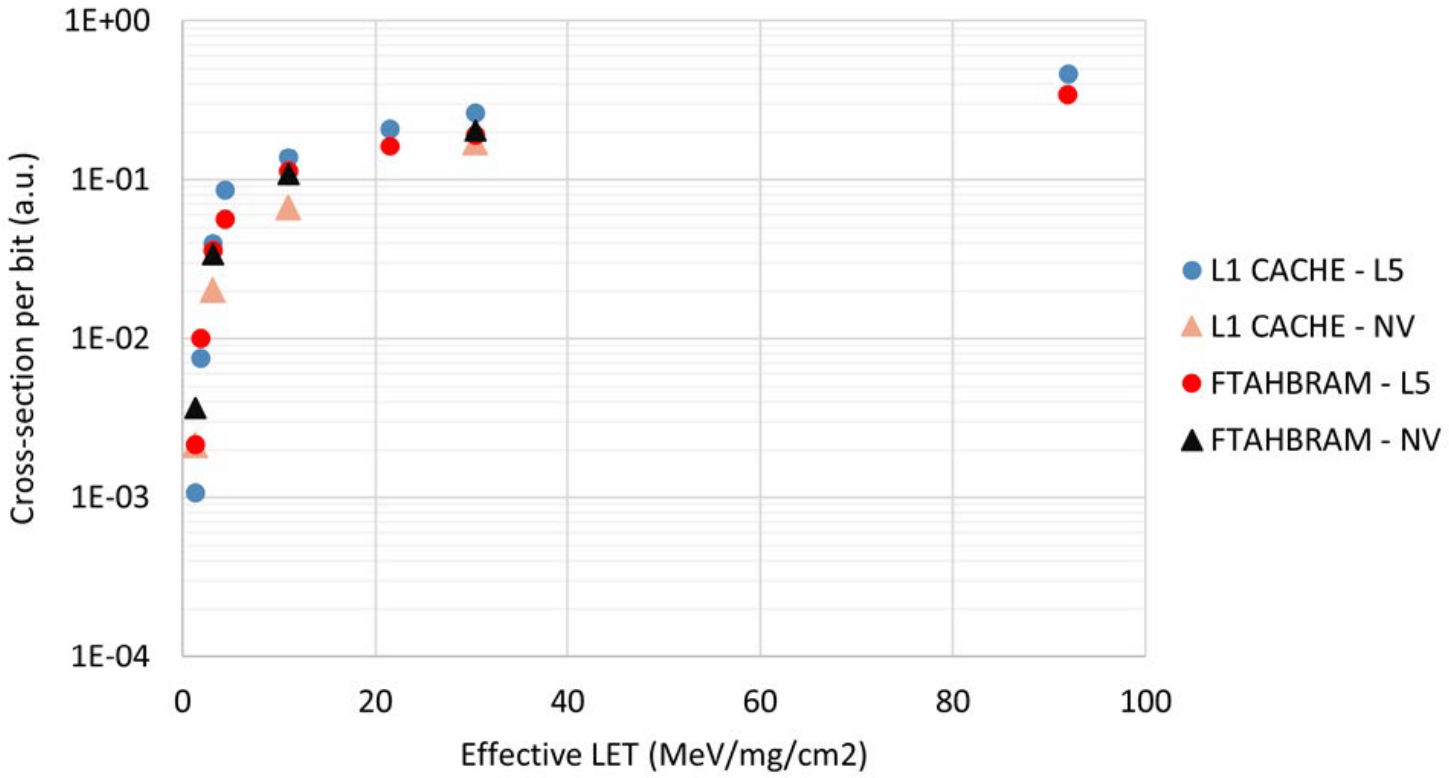
* VBODY are upper and down values. For instance, 1100 represents +1100mV and -1100mV.

NOEL-V summary results

- No SDCs
- No SEFIs
- All errors detected in the memories (FTAHBRAM and L1 cache) were corrected by the fault-tolerant features of the processor/device
- No SEL-like events (tests performed at room temperature)

SEE results – Heavy ions

All detected errors in memories (FTAHBRAM and L1 cache) were corrected by the FT features of the processors/device



SEE results – Protons

NOEL-V (NV) and LEON5 (L5) processors tested at different frequencies and bias conditions

Target	Frequency (MHz)	VCORE (mV)	VBODY* (mV)	Description
NV/L5-HP1	1000	1100	1100	NV and L5 high performance, maximum VCORE
L5-HP2	1000	900	1100	L5 high performance with lower VCORE
L5-HI	500	1100	1100	L5 from HI test
L5-GX	500	900	0	L5 medium frequency, low core voltage, low leakage body bias (0 V)
NV-HI	400	1100	1100	NV from HI test
NV-GX	400	900	0	NV low core voltage, low leakage body bias (0 V)
NV/L5-LP	250	670	0	NV and L5 low performance with lowest VCORE

* VBODY are upper and down values. For instance, 1100 represents +1100mV and -1100mV.

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SEE results – Heavy ions

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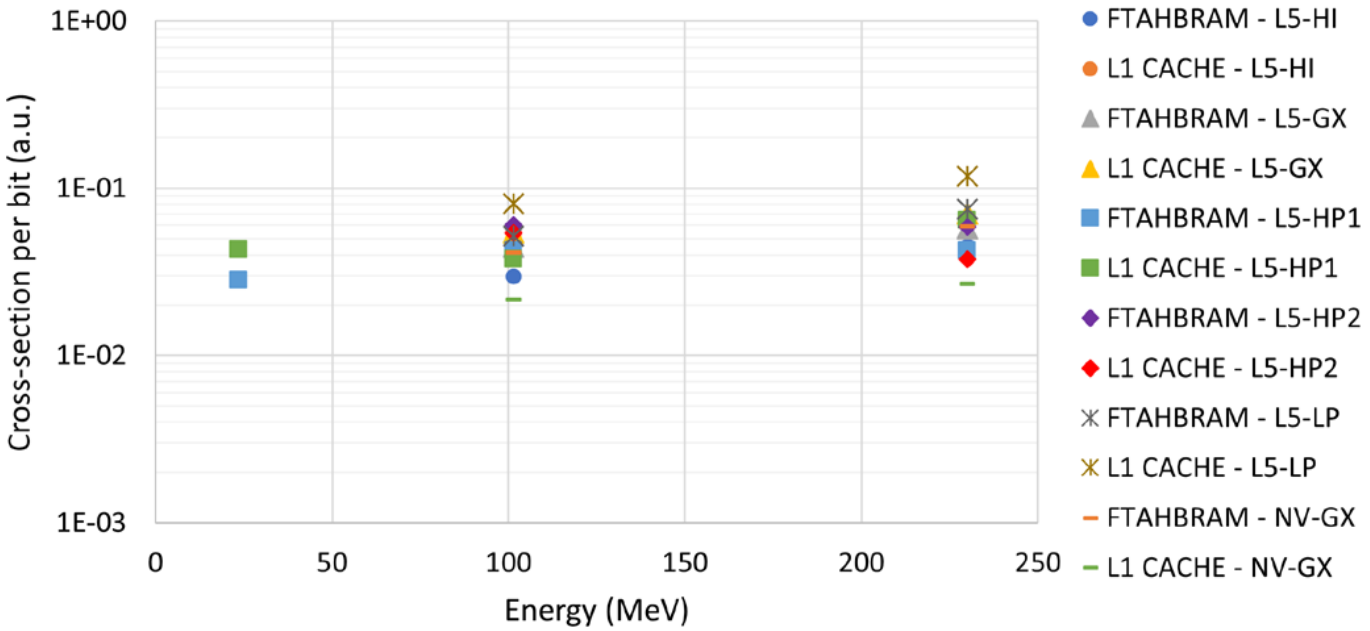


06

Conclusions

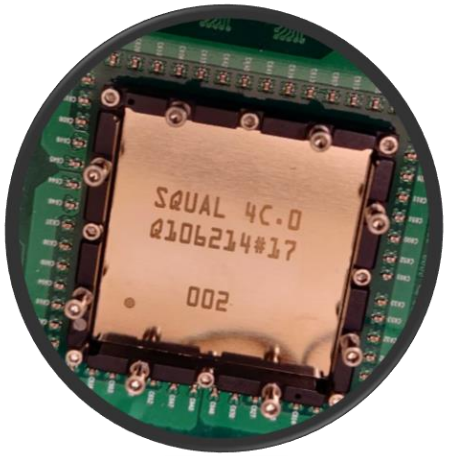
Conclusions

- **Radiation-hardened demonstrator with NOEL-V 64-bit RISC-V and LEON5 32-bit SPARC V8 processors**
  - Flip-flops and combinational logic hardened via standard cell libraries from STMicroelectronics' 28nm FD-SOI GEO P2 platform for Space
  - Following this tape-out, several updates were performed in the processors for the final **GR765 SoC**

- **Technology hardness and processor cores' fault tolerance features demonstrated through SEE test campaigns**

- **No functional events observed**
- **All events detected in the memories (FTAHBRAM and L1 cache) were corrected by the fault-tolerant features of the processor/device**
  - No uncorrectable events detected
  - No need for lock-step or redundant processors

- **SEE rates for correctable memory events***
  - L1 cache correctable events: 1003 days in LEO and 787 days in GEO
  - FTAHBRAM correctable events: 197 days in LEO and 141 days in GEO



* TRAD Omere 5.5 software, Heavy ion and Proton data, AP8 solar min for trapped protons, ESP for solar mean protons, Z = 1-92, CREME96 for heavy ions, 1 g/cm² Al shielding, 0.01 µm cell depth.
Cell area: 0.18 µm² for FTAHBRAM and 0.47 µm² for L1 cache

THANK YOU!

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