Ready for Launch

MICROCHIP

A Leading Provider of Smart, Connected and Secure Embedded Solutions

RISC-V IN SPACE

SMART | CONNECTED | SECURE

Ted Speers

April 2, 2025

Key Messages

- RISC-V® and space have been linked at Microchip from day one.
- Huge strides have been made in the last decade.
- The space market matters.
- An exciting future lies ahead for RISC-V® in space.

Theme of the Day — Flywheels

Notice:
- RISC-V and the RISC-V logo are trademarks of RISC-V International.
- Use of these trademarks is for informational purposes only and does not imply affiliation or endorsement .

RISC-V® Summit Keynote: 2019

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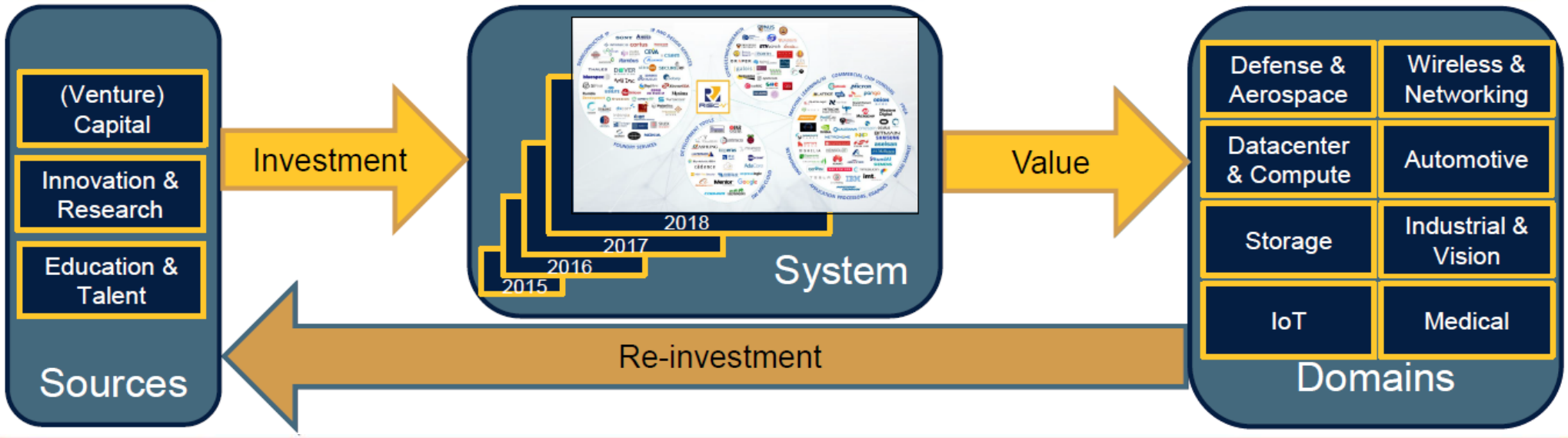
"The speed of evolution here is mind-blowing."



~2015 – I become RISC-V® Aware

MICROCHIP

December 11, 2014

December 8 - 12, 2014

THURSDAY

11

6 AM

7

8

9 **Bruhnspace Telephone Call - Auburn Conf Room**
SiSoC Auburn "Executive" (B1)(FL2)(10)

10

- **~10:25am**
  - I become RISC-V Aware
- **~10:35am**
  - I check out www.riscv.org

~2015 – I become RISC-V® Aware

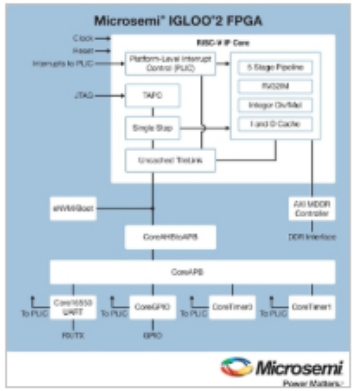
BruhnBruhn Innovation

BruhnBruhn Innovation is an engineering company that has evolved from the technical research conducted within Bruhnspace Holding (nowadays renamed to BruhnBruhn Holding). Founded in Sweden in 2012

Source: www.bruhnbruhn.com

2016 – Microsemi Introduces RISC-V® Soft-CPU

feature article



November 29, 2016

Microsemi Tackles RISC-V

Open Architecture FPGA Processor Core

by Kevin Morris

In many applications today, the combination of FPGA programmable logic fabric with a microcontroller is the magic sauce that brings the whole system together and makes it "smart." The flexibility in interface, communication, and peripherals provided by the FPGA part, along with the software-programmability of a microcontroller, truly delivers on the promise of the system-on-chip "SoC" moniker for a number of smaller-scale systems.

Source:www.eejournal.com

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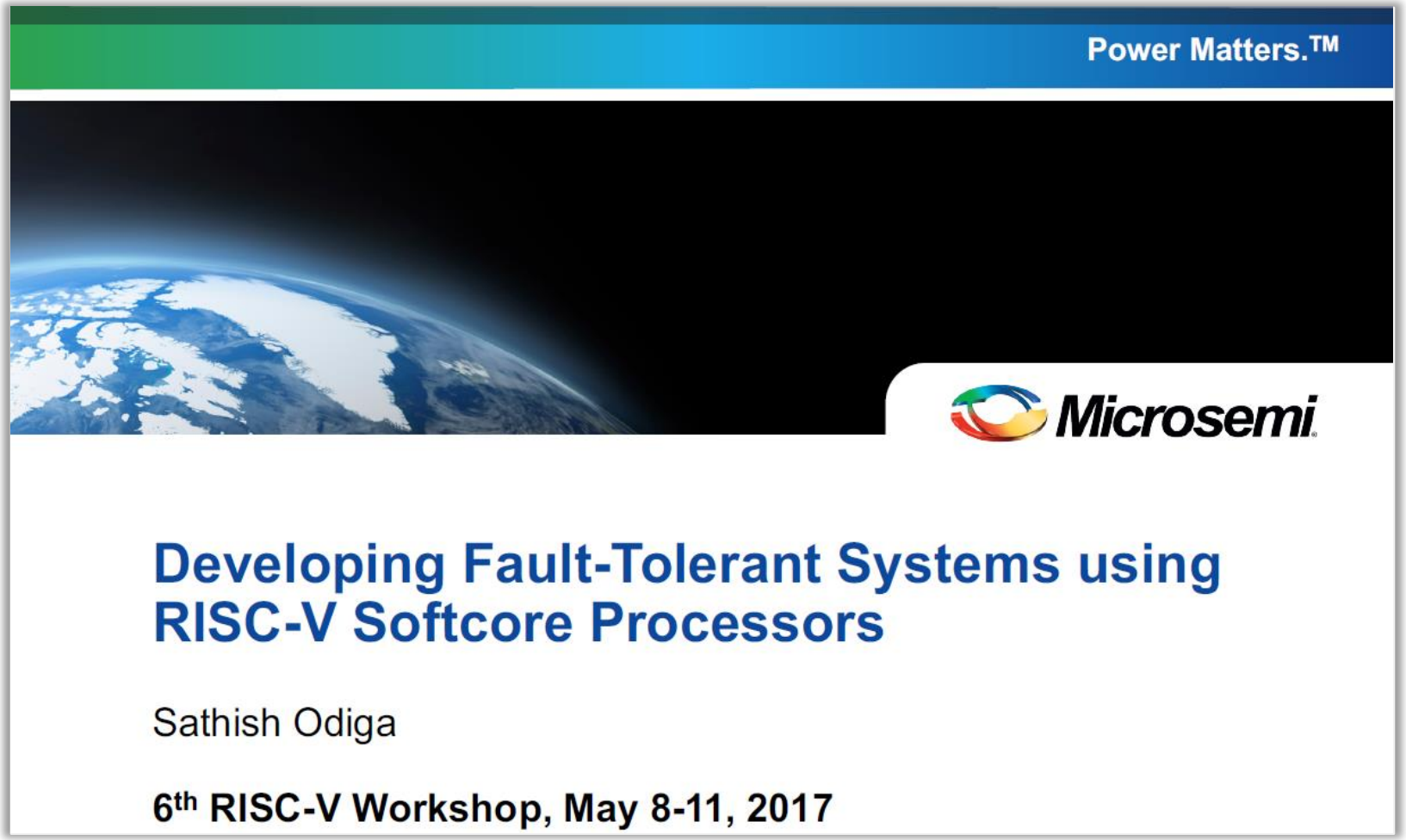
2017 – The real reason we took the plunge reveal

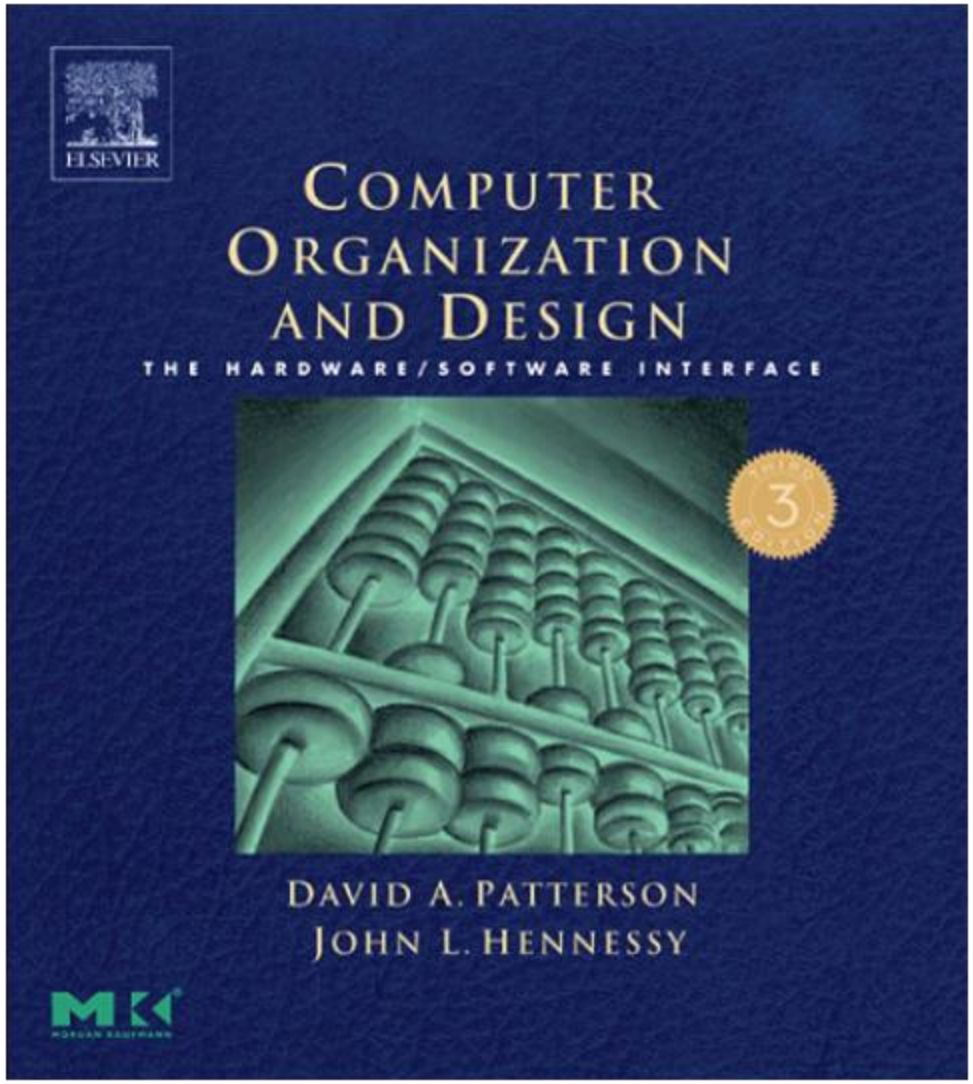


2017 – The real reason we took the plunge reveal

RISC-V Processor Advantages

- RISC-V open source licensing provides flexibility to customize your processor for safety-critical requirements
  - Processor internal memory blocks protection using SEC-DED
  - Bus interfaces protection using error correcting codes
  - Block level hardware redundancy for error detection/correction
  - Selective hardening
  - Hardware based checkpointing and rollback
  - Logic optimization for performance
- Extensible ISA
- Portability
  - Platform independent RTL
- Security due to open source ISA
  - Deep inspection of source code builds trust

2017 – RISC-V® and Education



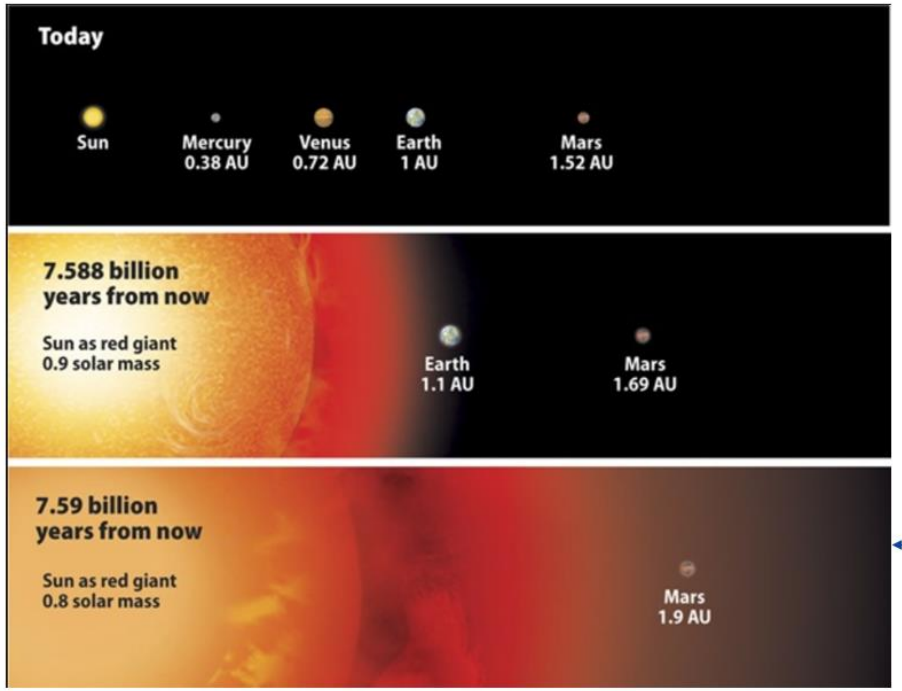
2017 – RISC-V® and Education

RISC-V® is the lingua franca of computer architecture education and research.

2019 – Keynote FPGA Forum

2019 – Keynote FPGA Forum

Bad Day for Earth



Dec 3, 7,590,002,019

Astronomy: Roen Kelly, after Klaus-Peter Schroeder and Robert Cannon Smith

2019 - Keynote FPGA Forum

… But Not Necessarily for RISC-V

NASA

SPACEX

esa

Our Team v. These Guys

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Defining the Edge – RISC-V® Workshop 2019

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Edge of the Troposphere

~200,000 flights a day tracked by FlightRadar24

8

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Defining the Edge – RISC-V® Workshop 2019

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Edge of the Solar System

View of Pluto as *New Horizons* left the system, catching the Sun's rays passing through Pluto's atmosphere, forming a ring.

Image source: NASA

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Defining the Edge – RISC-V® Workshop 2019

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Edge of the Universe

Galaxy **GN-z11**, shown in the inset, is seen as it was 13.4 billion years in the past, just 400 million years after the big bang, when the universe was only 3 percent of its current age.

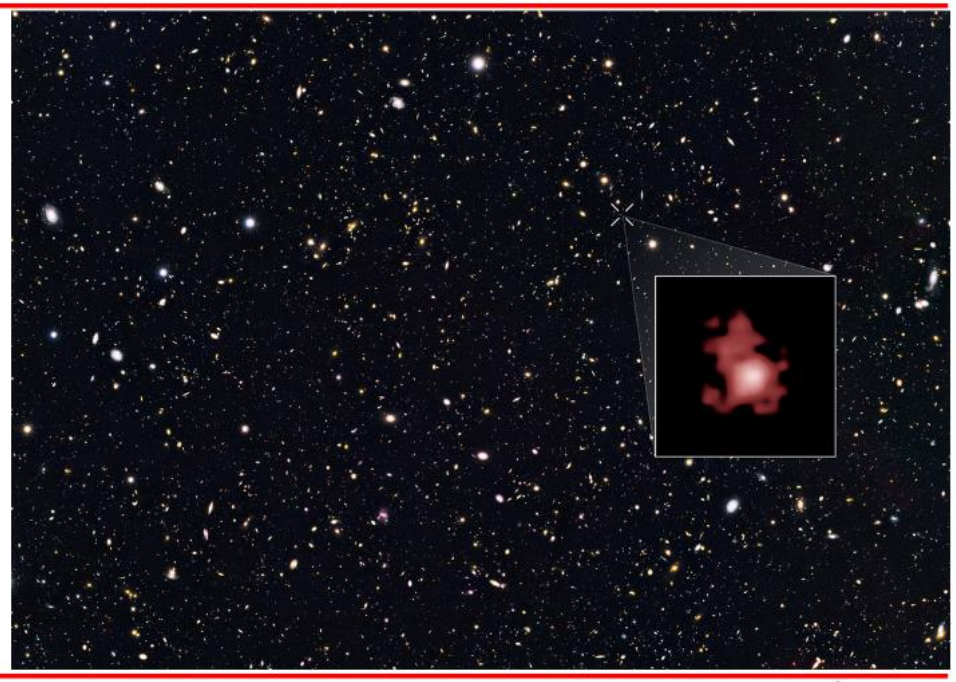

Image source: NASA

6

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Defining the Edge – RISC-V® Workshop 2019

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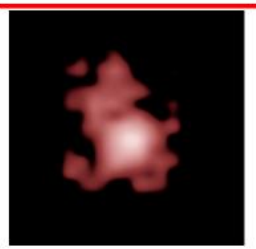
Microchip FPGAs at the EDGE

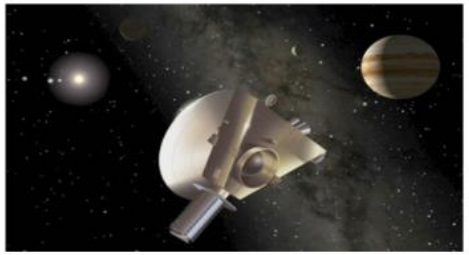
Boeing 787 Dreamliner

Pluto New Horizons
Pluto Images 2015



Hubble SM-4
WFC3 Install 2009

APA, A3P, AX



RTSX32SU, RTSX72SU

RH1280

Image sources: NASA

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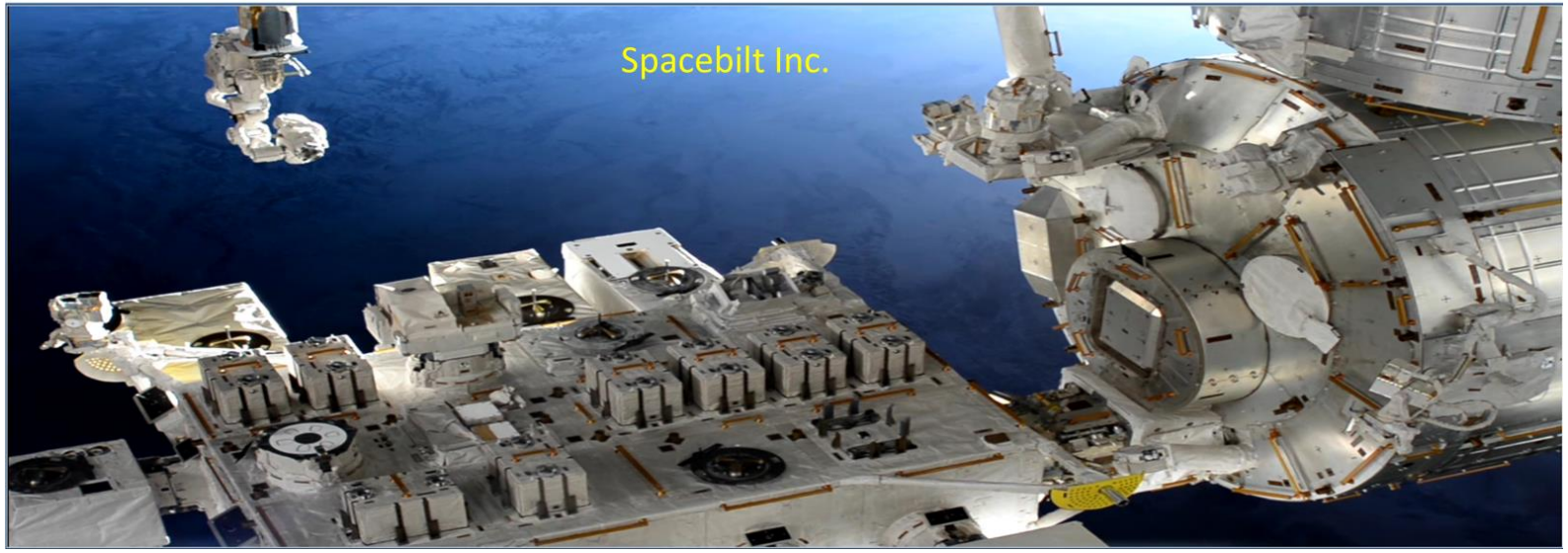
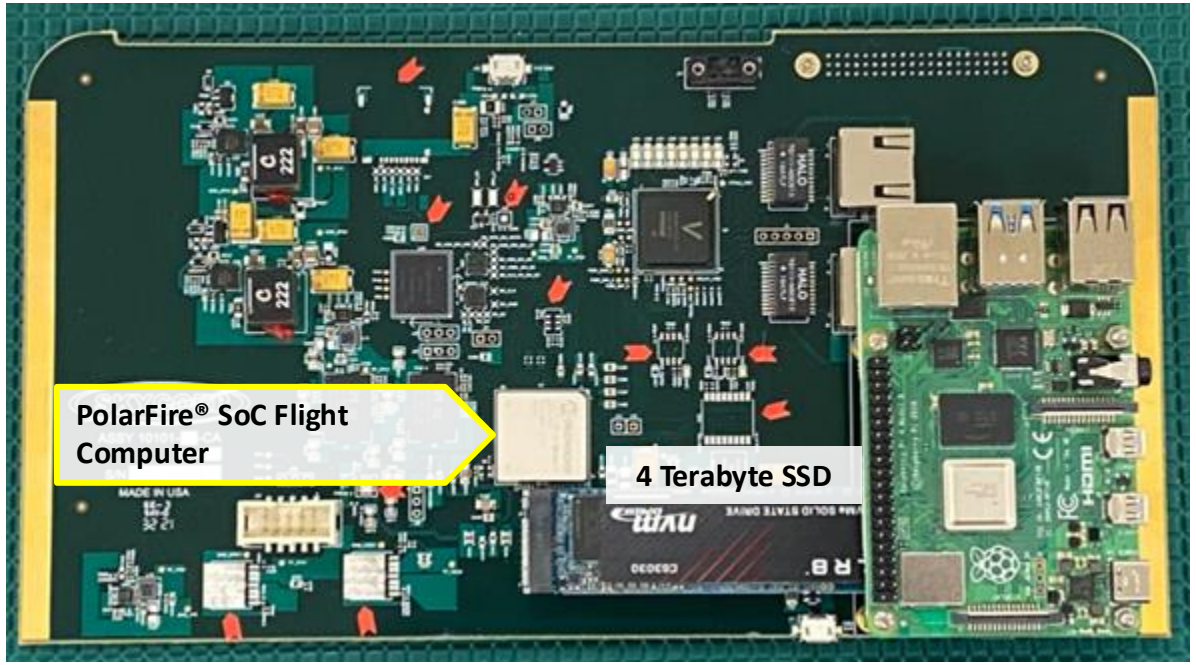
2021 Space Computing Conference

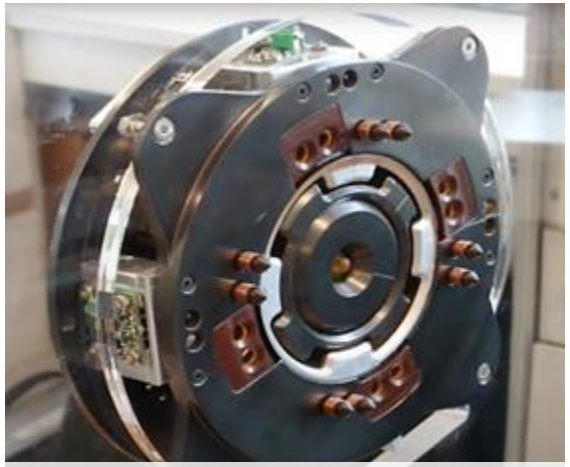
2022 – RISC-V® to the ISS

PolarFire™ SoC In Space



ISSF Mission to ISS 2022



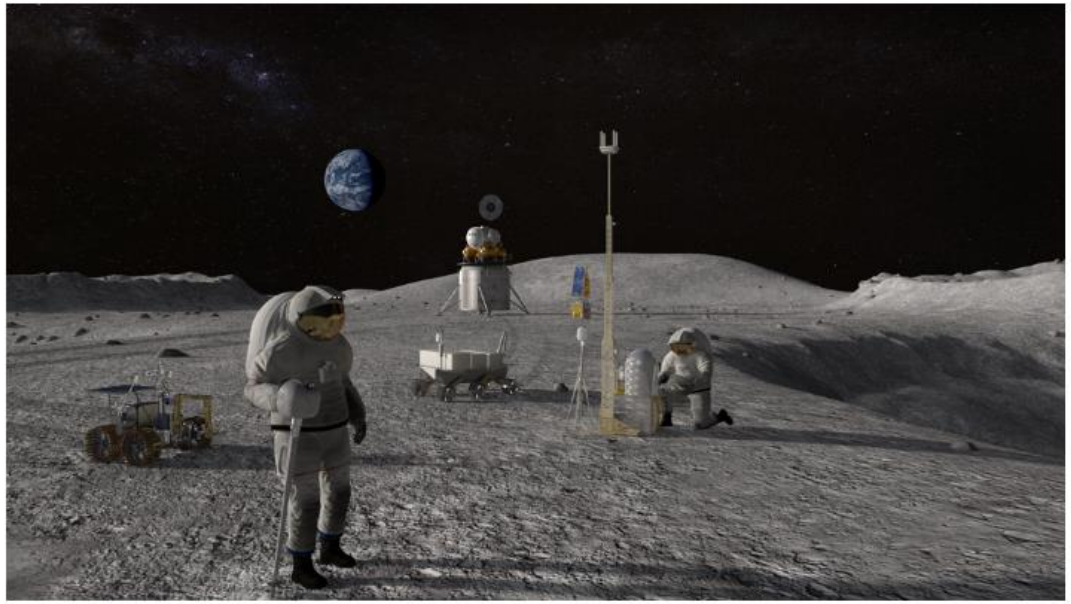

Intelligent Space Systems Interface


iSSIFQE Flight Hardware

Source: Used with permission by SpaceBilt

2022 – Microchip Wins HPSC

NASA Awards Next-Generation Spaceflight Computing Processor Contract



NASA's Jet Propulsion Laboratory has selected Microchip Technology Inc. to develop a high-performance spaceflight computing processor that will support future space missions. **Credits: NASA**

Source: www.nasa.gov

2022 – Microchip Wins HPSC

As part of NASA's ongoing commercial partnership efforts, the work will take place under a $50 million firm-fixed-price contract, with Microchip contributing significant research and development costs to complete the project.

Source: www.nasa.gov

2024 – HPSC Launch – Space Computing Conference

Feature Highlights

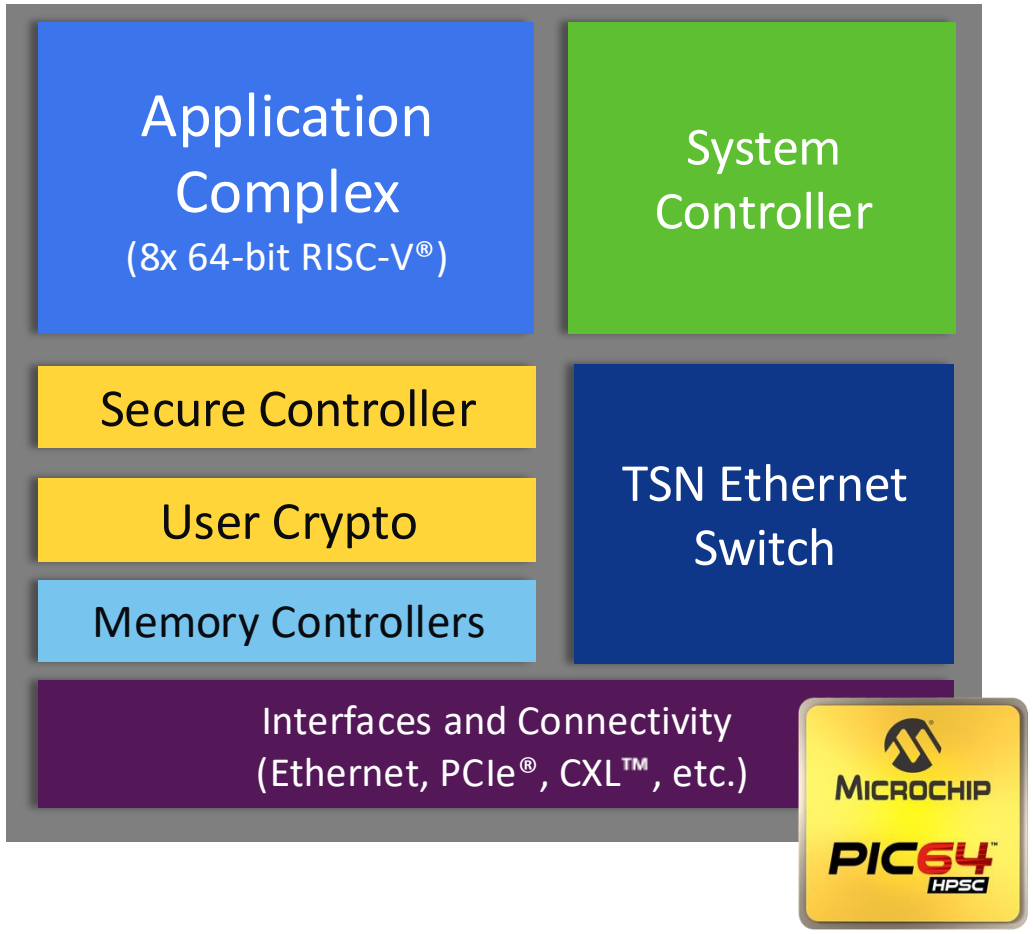
Radiation-Hardened and Radiation-Tolerant Versions Enable a Spectrum of Mission Profiles

Compute

Groundbreaking **64-bit RISC-V © Vector** processing with virtualization targeting Edge AI (SiFive X288/X280)

Security

Defense Grade Security Enclave supporting **Post-Quantum** Cryptographic algorithms



Fault Tolerance

Unprecedented **Fault-Tolerance** capabilities for Mission Critical Applications (DCLS, Split-Mode, WorldGuard)

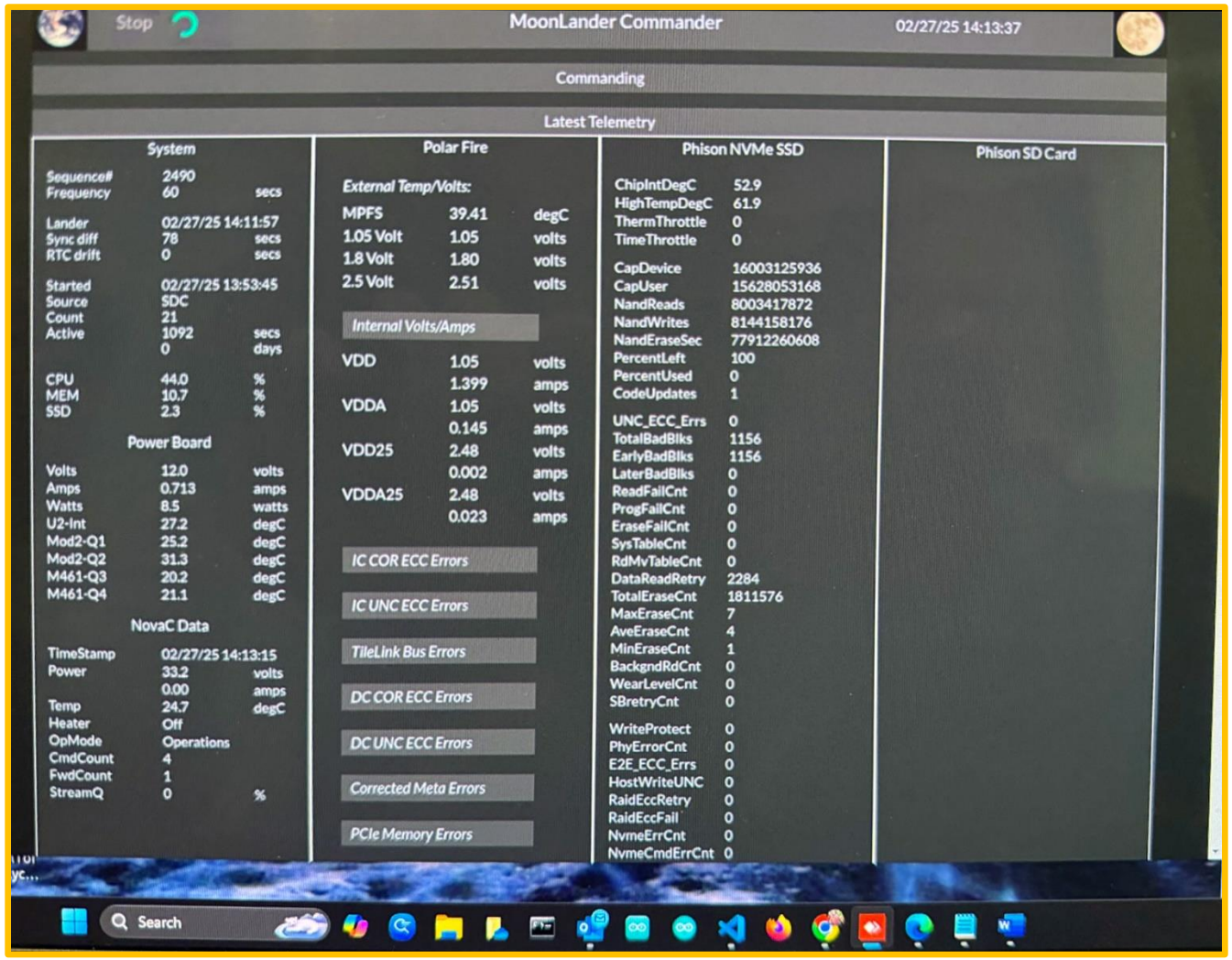
Massive Connectivity

Integrated **240G TSN Ethernet** Switch, **10GbE**, **PCIe**/CXL and **RDMA** for Networking & Deterministic Connectivity

MICROCHIP

2025 – RISC-V to the Moon

2025 – RISC-V® to the Moon



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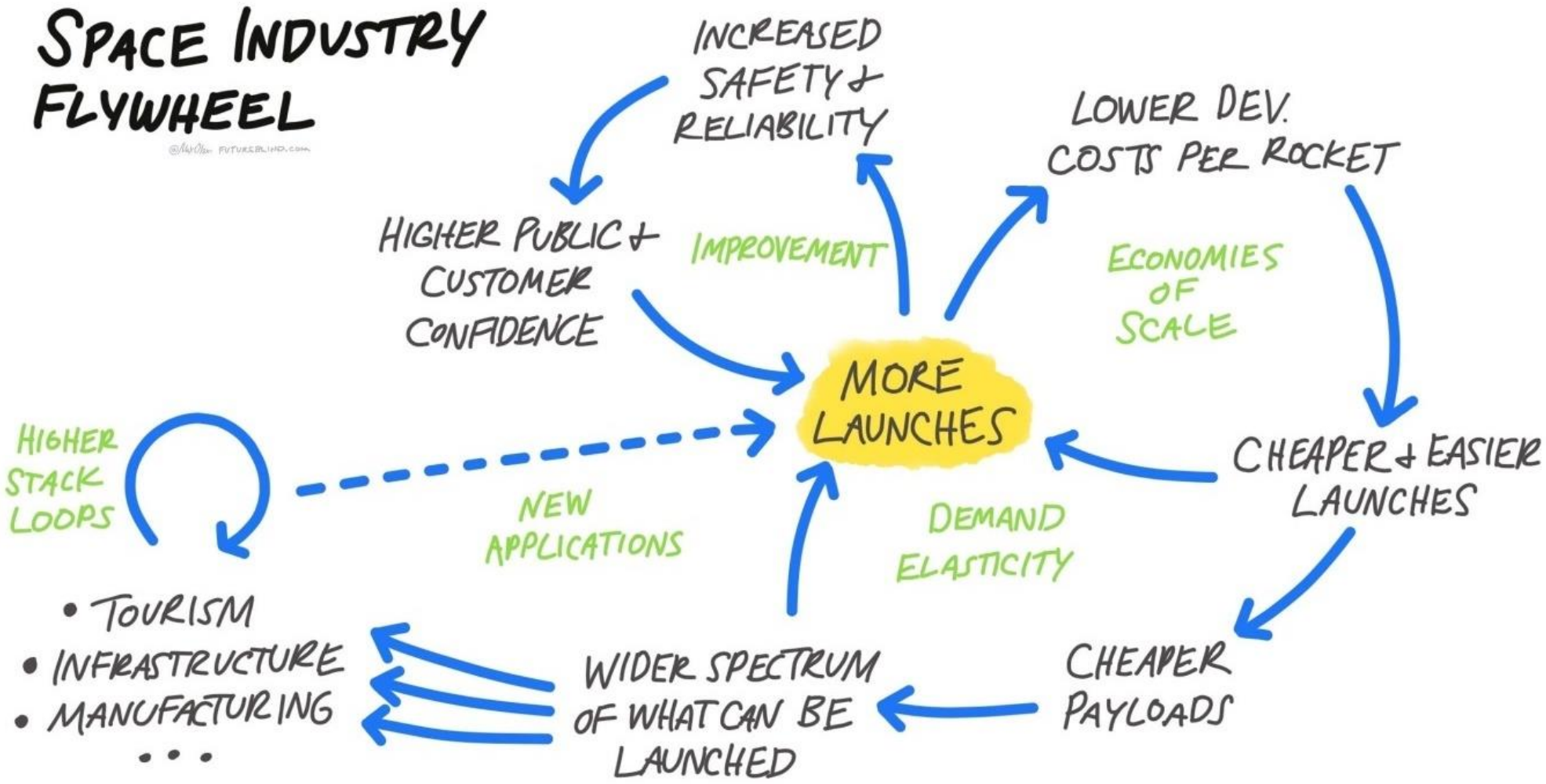
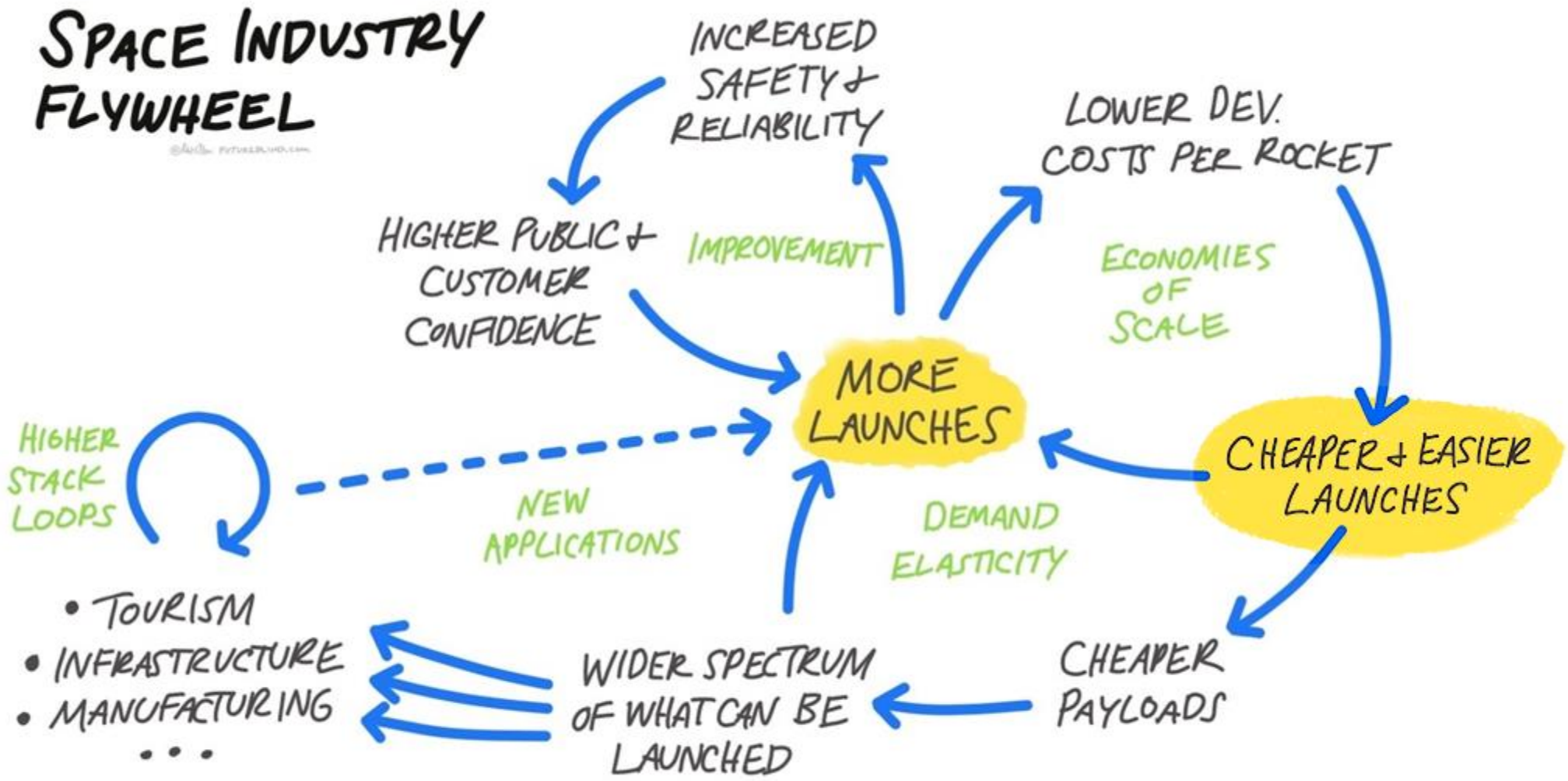
Flywheels Everywhere



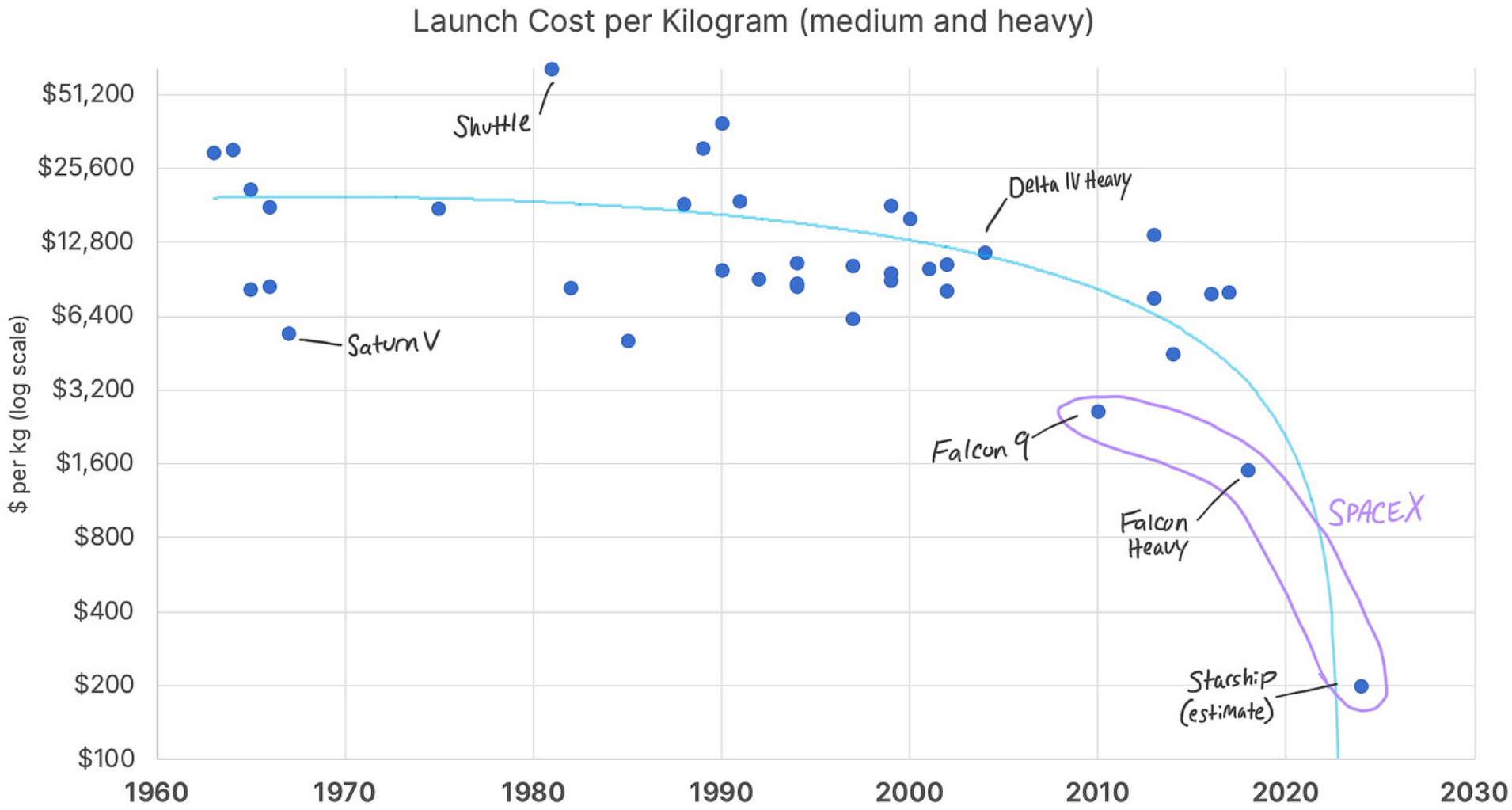
Source: https://futureblind.com/p/the-future-of-space-1

Flywheels Everywhere



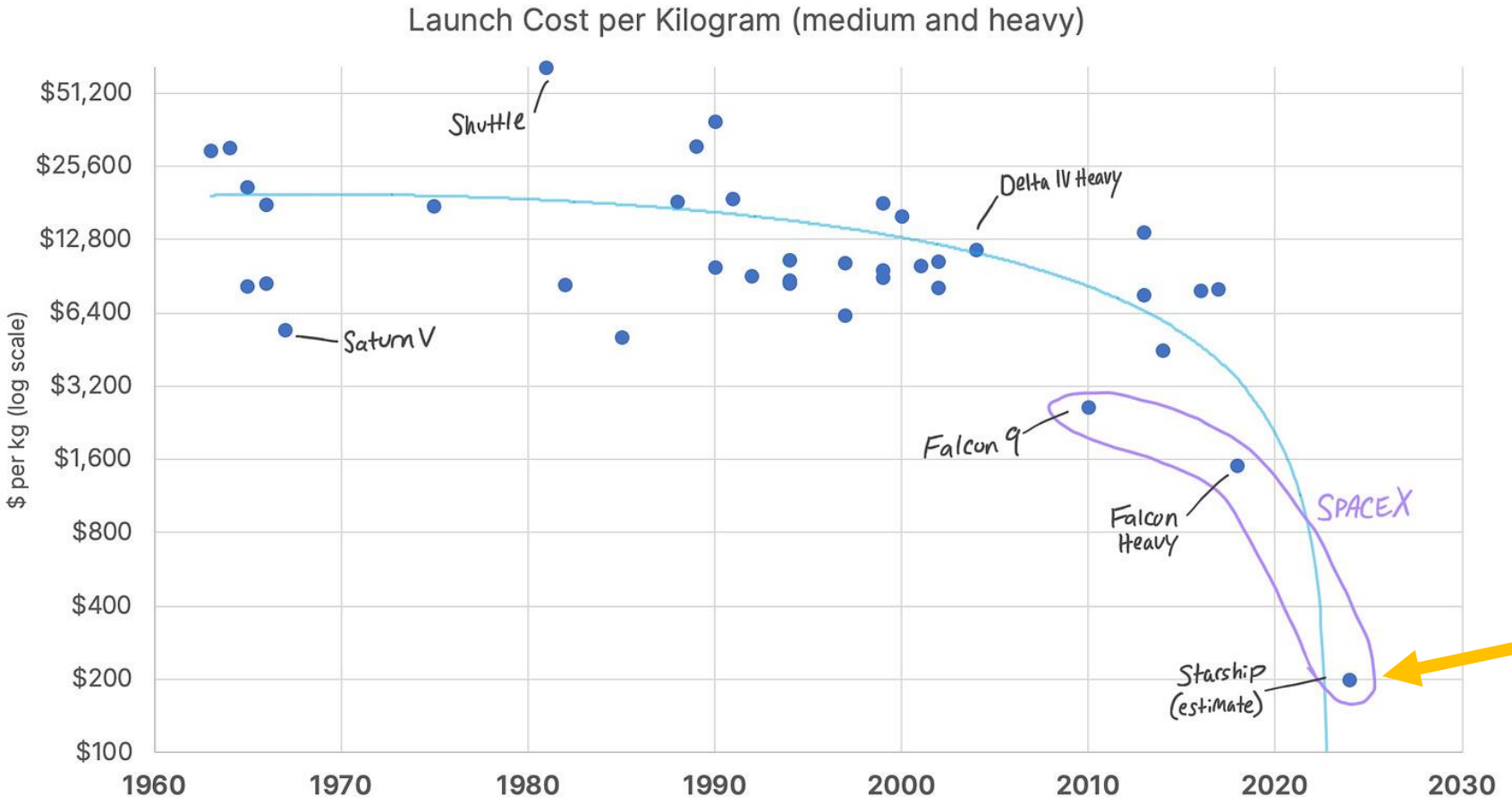
Source: https://futureblind.com/p/the-future-of-space-1

Fueling the flywheel – lower launch costs



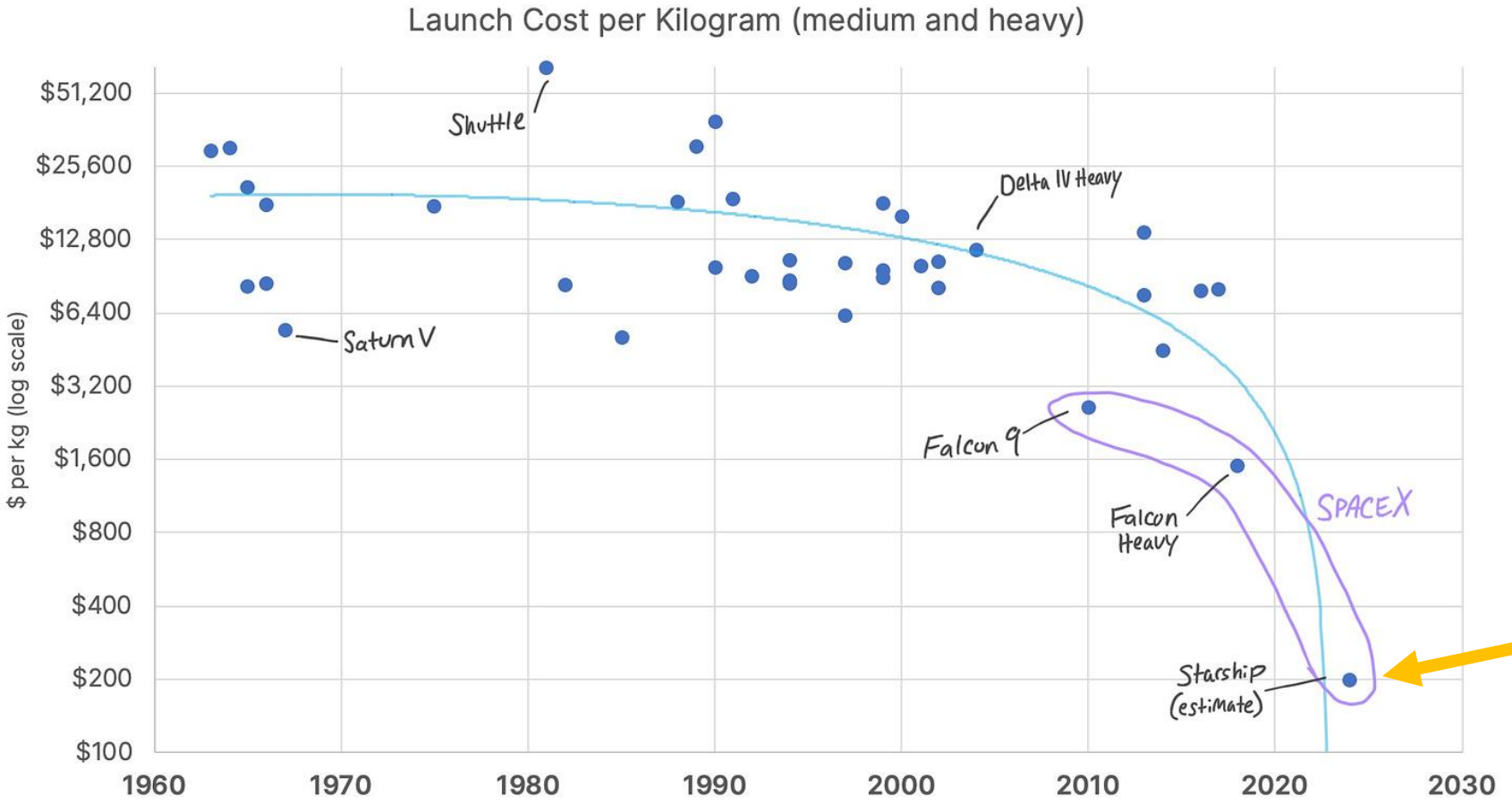
Launch cost image: https://futureblind.com/p/the-future-of-space-1

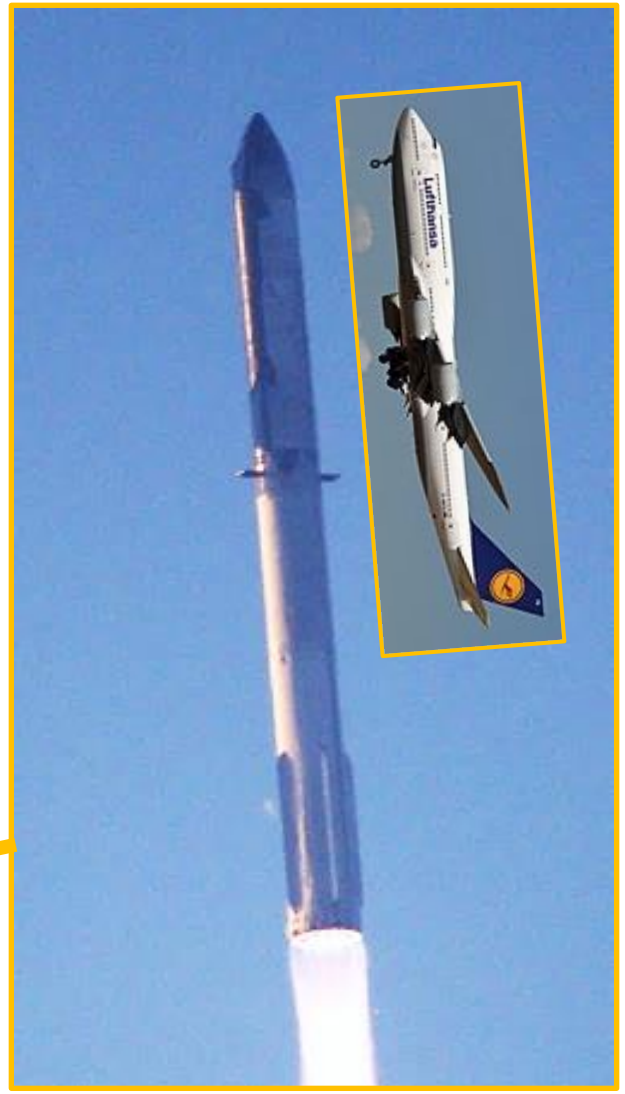
Fueling the flywheel – lower launch costs



Launch cost image: https://futureblind.com/p/the-future-of-space-1
Cropped starship image By Osunpokeh - Own work, CC BY-SA 4.0, https://commons.wikimedia.org/w/index.php?curid=141195403

Fueling the flywheel – lower launch costs





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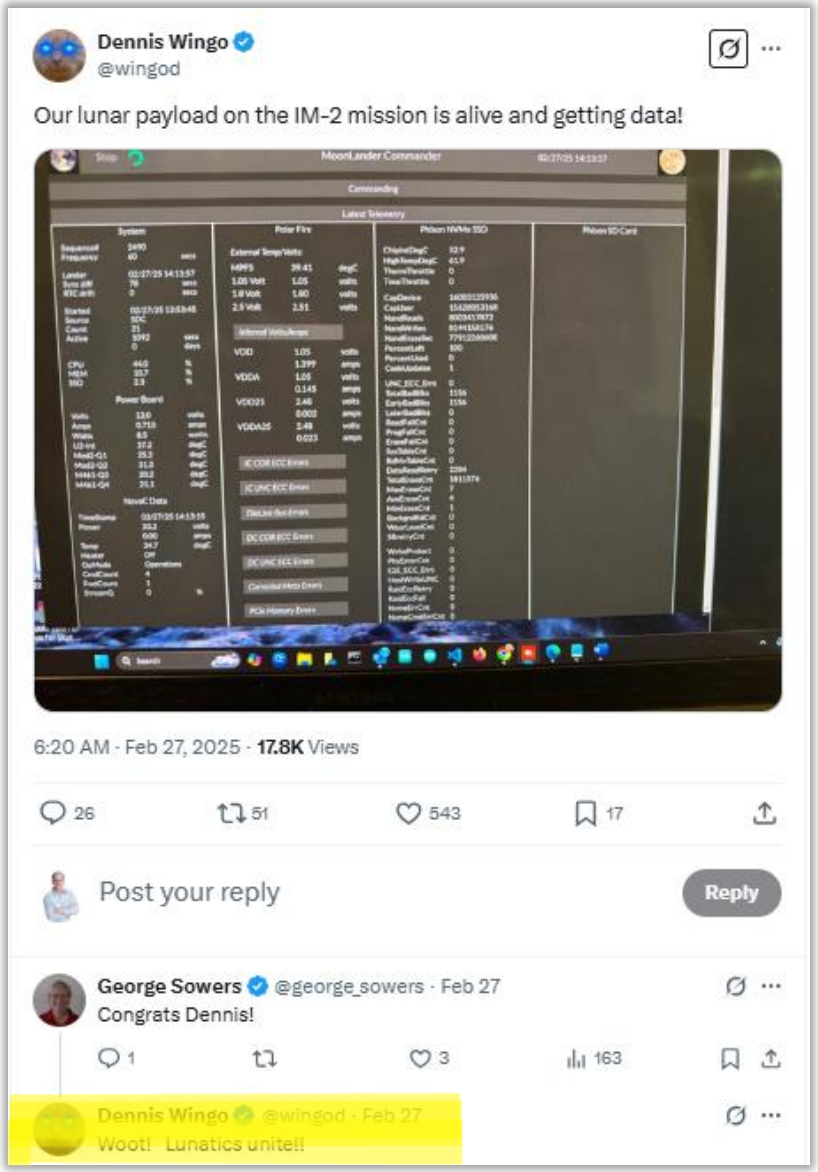
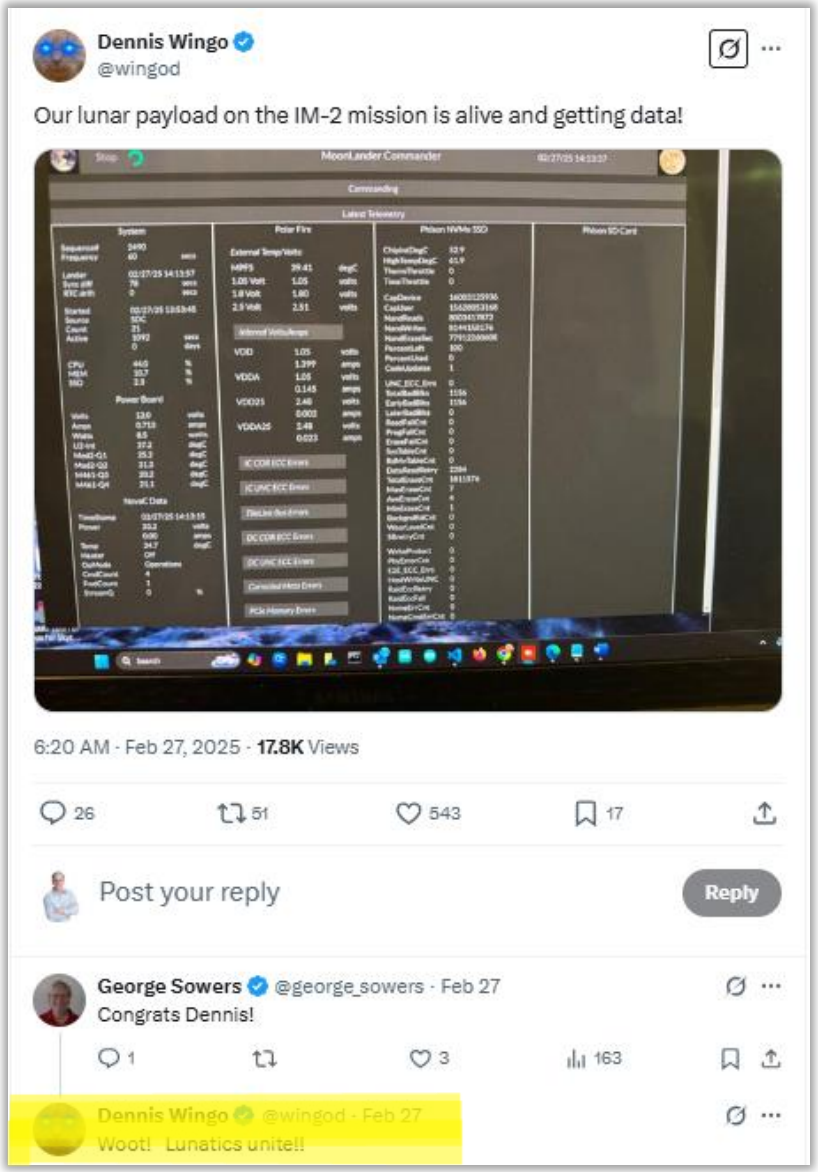
Cropped starship image By Osunpokeh - Own work, CC BY-SA 4.0, https://commons.wikimedia.org/w/index.php?curid=141195403

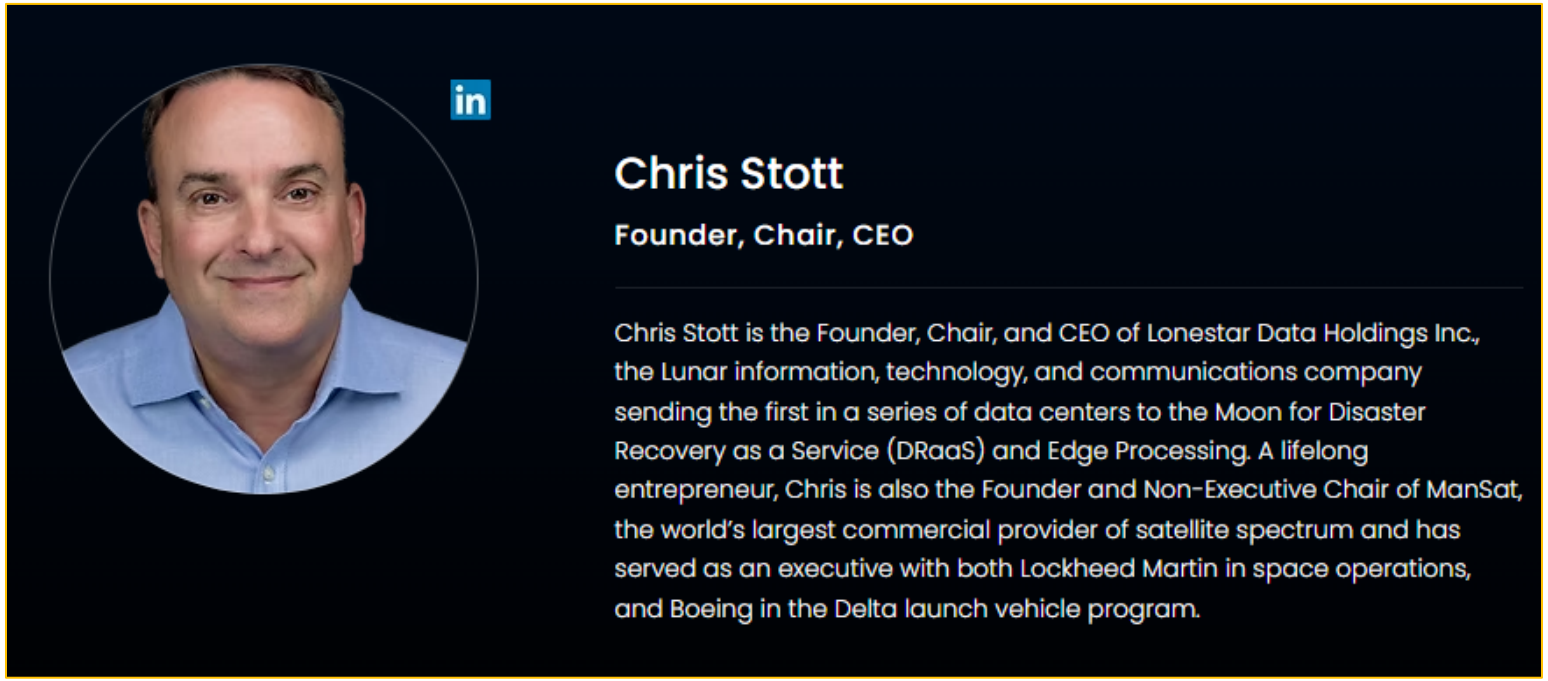
747 image By Anna Zvereva from Tallinn, Estonia, CC BY-SA 2.0, https://commons.wikimedia.org/wiki/File:Lufthansa,_D-ABYQ,_Boeing_747-830_(19014608834)_(3).jpg

Mix in some ‘lunatics’



Mix in some ‘lunatics’



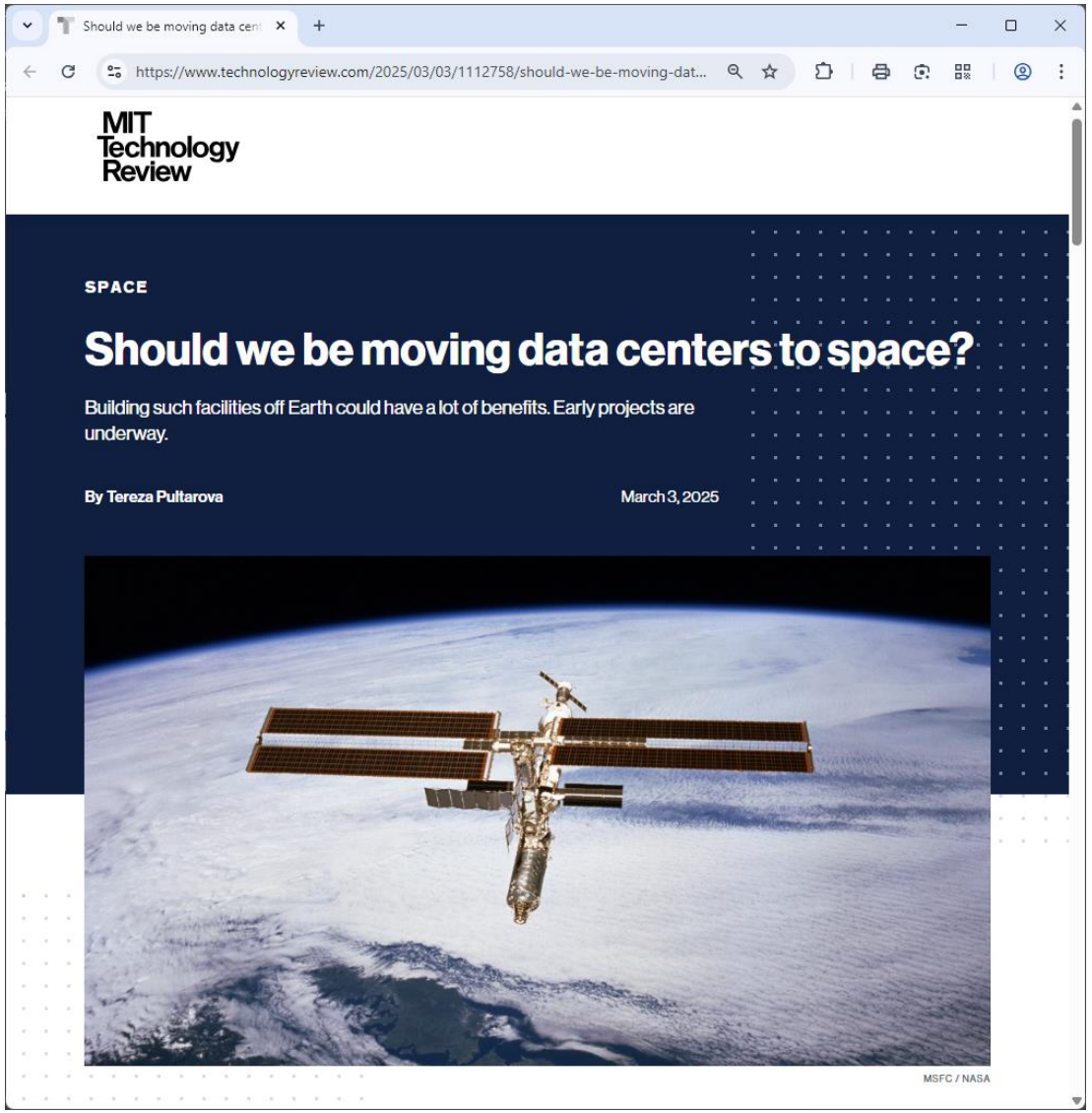


“Lonestar is working to save all our data … on the moon.”

“A place so ideal for global data storage that if it wasn’t there, we’d have to build it.”

Source: www.lonestarlunar.com

Not lunatics after all?



Y Combinator
https://www.ycombinator.com › companies › starcloud

Starcloud: Data centers in space

Starcloud is building a network of megawatt-scale data centers in space, scaleable to gigawatt capacity, to be able to train large models like GPT6.

TechTarget
https://www.techtarget.com › searchdatacenter › tip › Pr...

Projections and feasibility of data centers in space

Nov 8, 2024 — Data centers in low Earth orbit (LEO) could **save land use on Earth**, reduce energy costs due to solar power technology and reduce data latency.

European Space Agency
https://www.esa.int › Discovery_and_Preparation › Kno...

Knowledge beyond our planet: space-based data centres

Aug 5, 2024 — The first scenario involves **two satellites in the same orbit**, where one is collecting data and the other one acts as a space data centre. A ...

IBM
https://www.ibm.com › think › news › data-centers-space

Are data centers in space the future of cloud storage?

Nov 18, 2024 — We see data centers in space as **producing at least 10 times lower carbon emissions**, even including the launch," says Co-Founder and CEO Philip Johnston.

CNBC
https://www.cnbc.com › 2024/06/27 › europe-wants-to-...

Europe wants to deploy data centers into space, study says

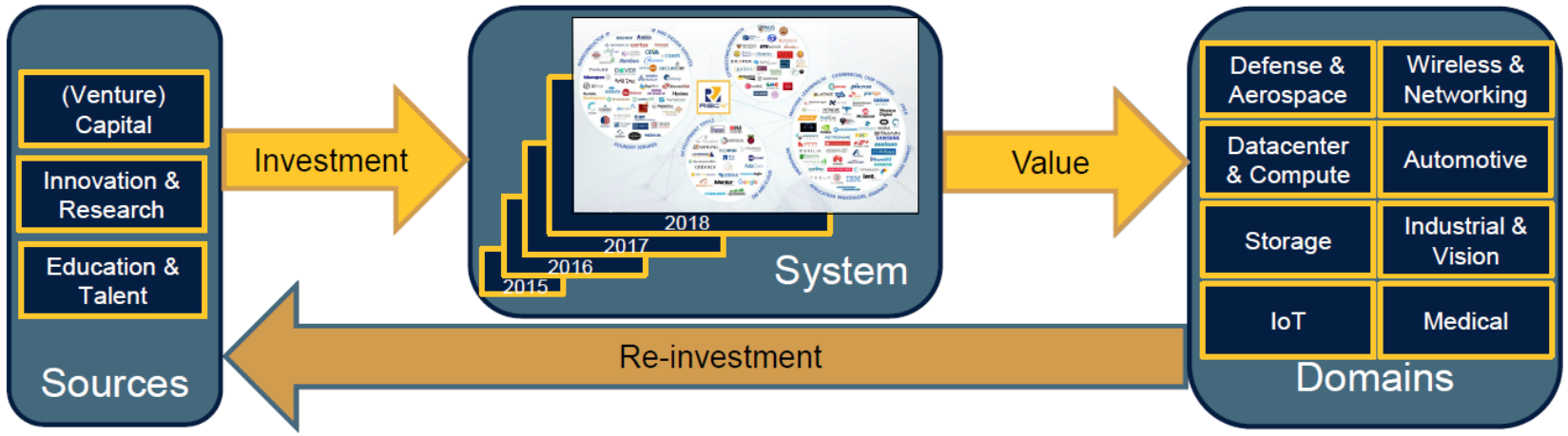
Jun 27, 2024 — **Europe is exploring the possibility of launching data centers**, which consume vast amounts of electricity, into space.

Source: www.technologyreview.com

Watch for it, it's (increasingly) all around you

Prediction: All commercial technology companies will develop space strategies.

The next spin around the flywheel … 2025 - …



Building a Best-in-Class Ecosystem

Single Board Computers

MOOG

SOSA SpaceVPX Compliant Extended 3RU

ibeos

SpaceVPX 3RU/6RU

IDEAS Engineering & Technology

SOSA SpaceVNX+ Compliant Mini SBC for Launch tubes, UAVs, and CubeSats

IPs / Services

MICROCHIP TSN, RDMA

DORNERWORKS

GROVF

Development Tools

Development Environment

MPLAB PRO IDE

MPLAB EXTENSIONS

Visual Studio Code

Compilers and AI Compilers

LLVM COMPILER INFRASTRUCTURE

GCC

MPLAB EXTENSIONS

OpenXLA IREE

Radiation Tolerant Silicon

MICROCHIP

64Mb xSPI NOR	100 MHz OSC	1000Base-T Single-PHY
64Mb Parallel NOR	156.25 MHz OSC	1000Base-T Quad-PHY
16Mb SRAM	Linear Regulator/LDO	RTG4, PolarFire, PolarFire2

TELEDYNE e2v Everywhereyoulook™

3plus

FRONTGRADE

RENESAS

infineon

Software, OS, Libraries

Operating Systems

Linux

RTEMS

SYSGO EMBEDDING INNOVATIONS

Xen Project

WNDRVR

Green Hills SOFTWARE

AI Frameworks

PyTorch

TensorFlow

TensorFlow Lite

Libraries

OpenSBI

OpenMP

FFTW

OpenSSL Cryptography and SSL/TLS Toolkit

$[Op\ BL]^T \times [en\ AS]$

Debuggers and Security

LAUTERBACH DEVELOPMENT TOOLS

ENTRUST SECURING A WORLD IN MOTION

MICROCHIP

Examples of HPSC Applications

Rovers

- Vision Processing
- Motion/Motor Control
- Nav Planning
- Science Instruments
- Communication
- Power Management
- Thermal Management
- Fault Detection/Recovery

Landers

- Hard Real-Time Compute
- High-Rate Sensors w/Zero Data Loss
- High Level of Fault Protection/Fail-Over

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PIC64™ HPSC

Satellites

- Platform and Payload
- Real-Time Sensor Data
- Non-Mission Critical
- High Bandwidth Sensors

Launchers

- Hard and Soft Real-Time
- Guidance and Control
- Autonomy and Crosslink Communication
- Sensor Data Processing
- Autonomous Science

Enables the Growing Need for Autonomy in Space Applications

PIC64HX – Target New Domains

PIC64HX High-Performance 64-bit MPUs

Enabling the Mission-Critical Intelligent Edge

Our PIC64HX product family represents a new class of high-performance, multi-core 64-bit microprocessors (MPUs) for aerospace and defense, industrial, automotive and communications applications. The PIC64HX MPU's architecture provides comprehensive Ethernet networking, advanced Artificial Intelligence and Machine Learning (AI/ML) processing and connectivity support while delivering unprecedented flexibility, fault tolerance, scalability and power efficiency.

Download the PIC64HX Brochure | Explore PIC64HX White Papers

Applications

Industrial

Aviation

Defense

Automotive

www.microchip.com/en-us/products/microprocessors/64-bit-mpus/pic64hx

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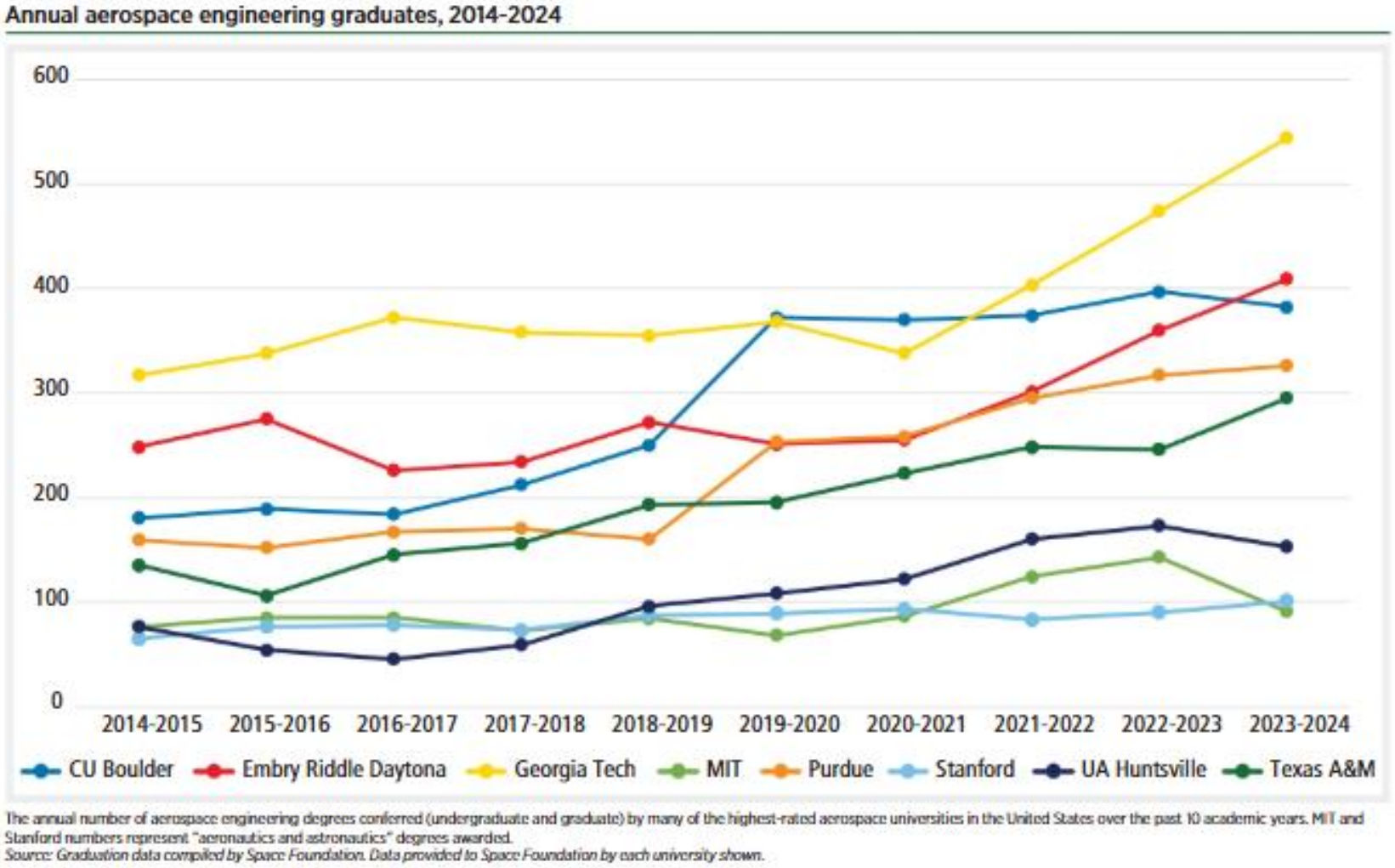
Strategic Imperative: Grow the Space Workforce

Enrollment up 50% over the last five years at Georgia Tech



Source: National Space Foundation Space Report

Teaching Computing with RISC-V® ➔

Computer Architecture at University of Notre Dame converted to RISC-V® in 2023

			Unit 1: Computing Performance and RISC-V
Unit Objectives: 1. **Describe** the fundamental components required in a **single core** of a modern microprocessor as well as how they interact with each other, wi 2. Suggest, compare, and contrast potential **architectural enhancements** by applying appropriate **performance metrics**.			
1	No Reading Due - Start of Semester	Tu, 1/16	**00 - Introduction to Computer Architecture** [PPTX]
	Reading 01: Introduction **Due 1/18/24 at 11:00am** [Reading Materials]	Th, 1/18	**01 - ISA Review and RISC-V Intro** [PPTX]
2	**Reading 02: Performance and RISC-V Instructions** **Due 1/23/24 at 11:00am** [Reading Materials]	Tu, 1/23	**02 - Computing Performance** [PPTX]
		Th, 1/25	**03 - RISC-V Instructions Introduction** [PPTX]

Source: https://github.com/mmorri22/cse30321

➔ Teaching Space Computing with HPSC

Computing in Spaceflight: Inspiring and Training the Next Generation of IC Design Professionals

PIs: Matthew Morrison, Co-PIs: Peter Kogge, and Doug Thain, University of Notre Dame

“We will collaborate with the NASA Jet Propulsion Laboratory’s High-Performance Space Computing (HSPC) project, NASA JPL Leadership Team member Pete Fiacco, and Microchip, which is leading the development of the HPSC processor.

…

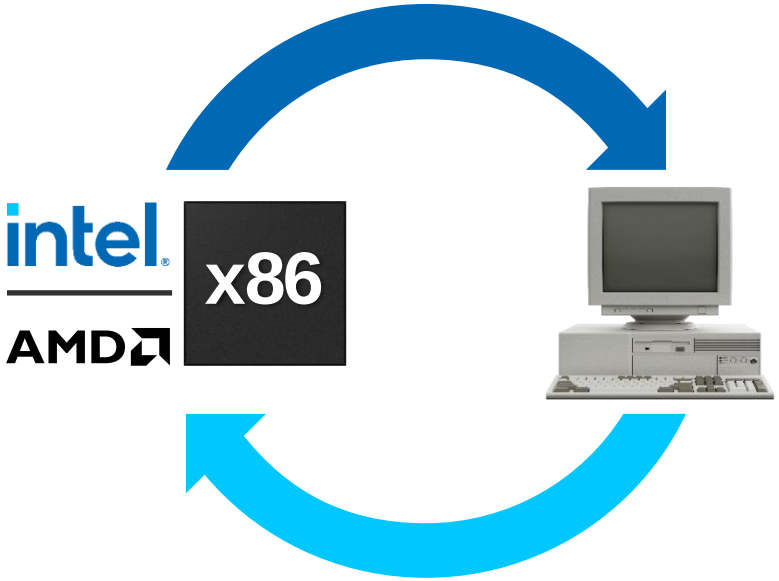
Integrating HPSC design principles into the proposed Computing in Spaceflight course will position those graduates at the cutting edge of innovative solutions for computing on space and on Earth.”

~2015 – I become RISC-V Aware

BruhnBruhn Innovation

"Courage is what makes BruhnBruhn who we are. By challenging your preconceived views and technology, we help you transform into something more than you expected."

Source:www.bruhnbruhn.com



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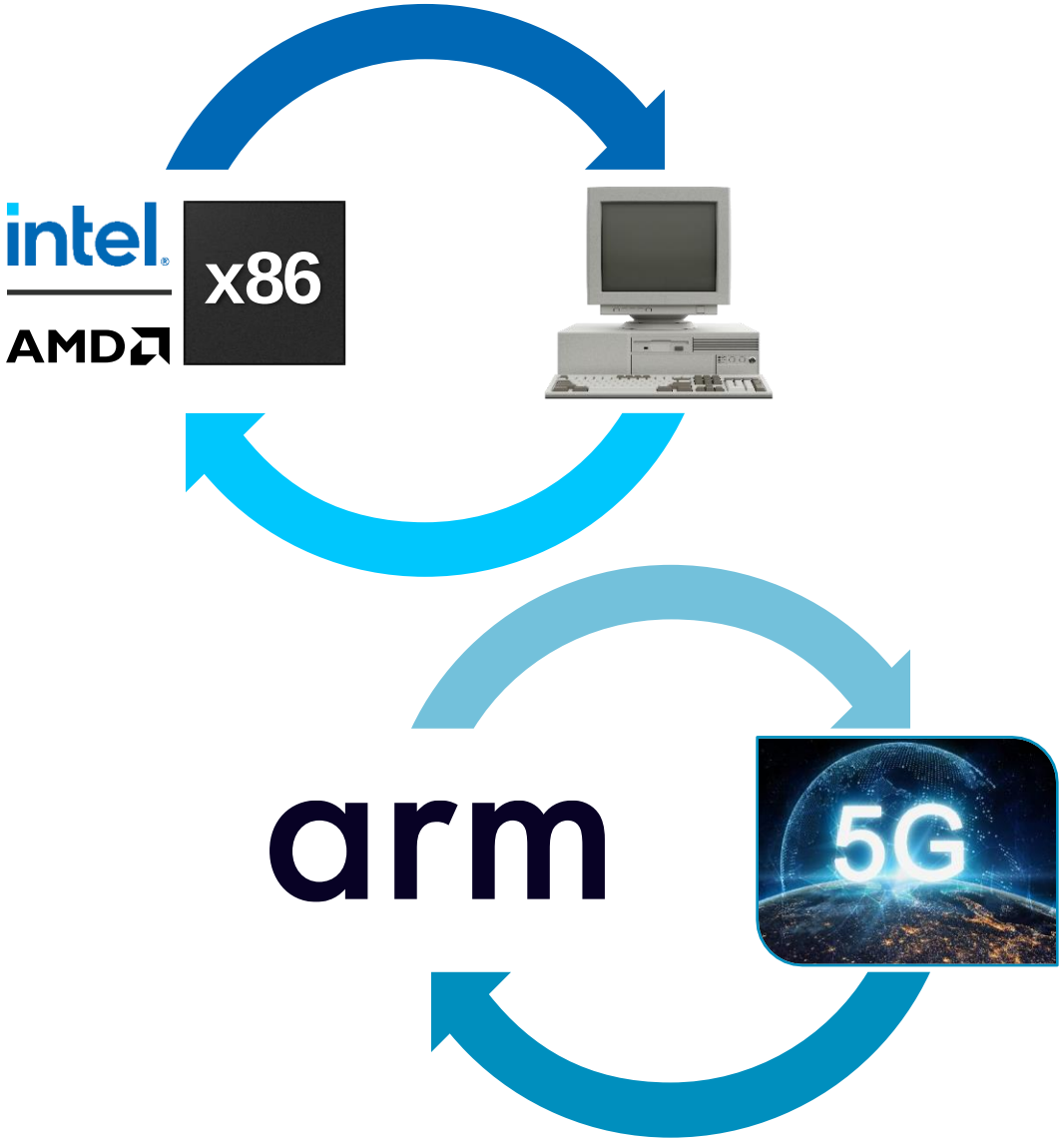

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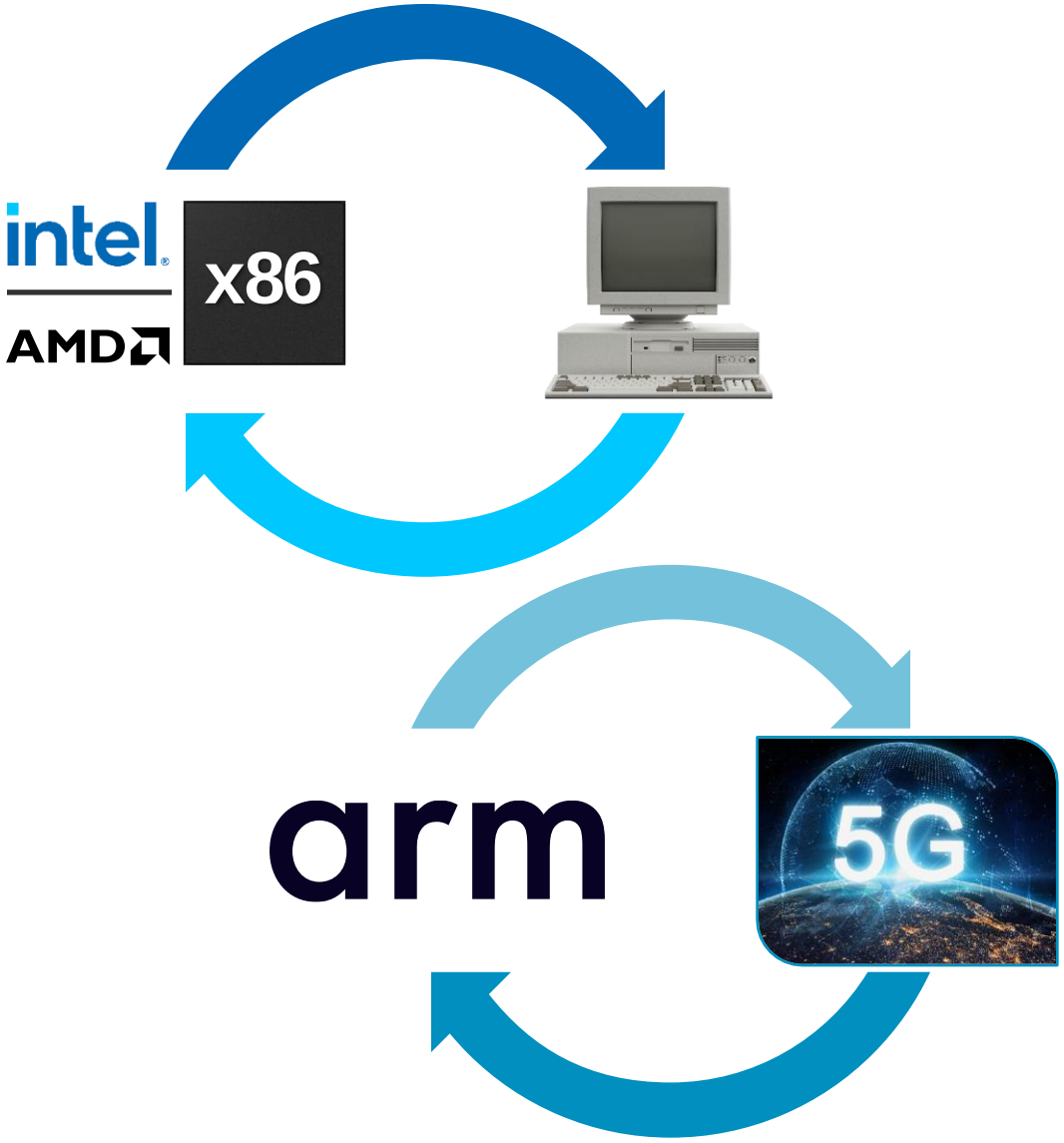
So Why Not?



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Lunatics and Really Big Flywheels

Modest RISC-V Project Goal

Become the industry-standard ISA for all computing devices

Krste Asanovic – Chief Architect

Lunatics and Really Big Flywheels

Modest RISC-V Project Goal

Become the **galactic** standard ISA for all computing devices

Ted Speers – Chief Lunatic

MICROCHIP

Thank You

MICROCHIP