DUROC Demonstrator in Rad-Hard N7 Technology

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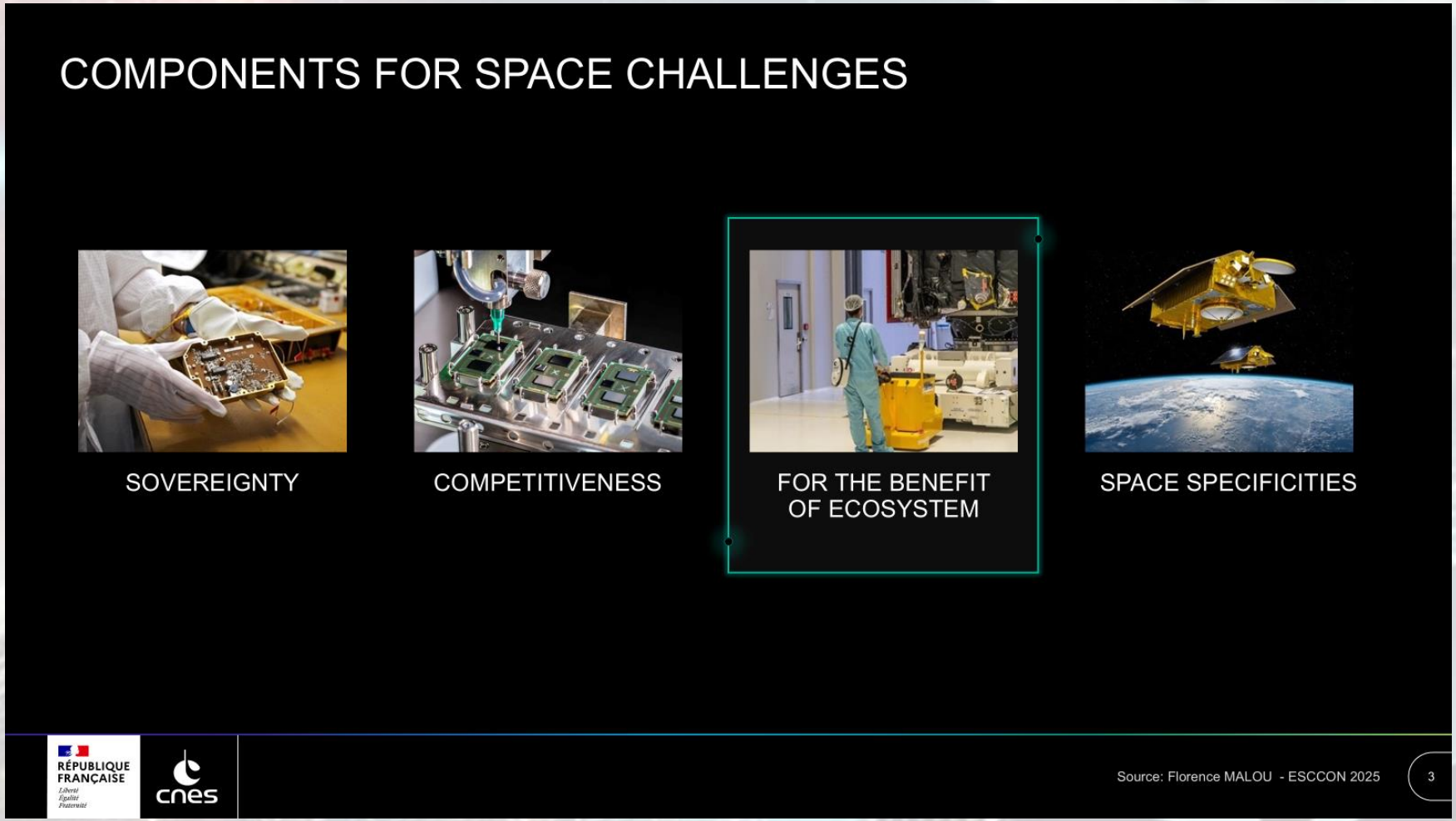
Alp KILIC

NanoXplore

This project has received funding from the European Union's Horizon 2020 research and innovation program under grant agreement N°101004206

Context in 2025 and Beyond



Courtesy of CNES (French National Space Agency)

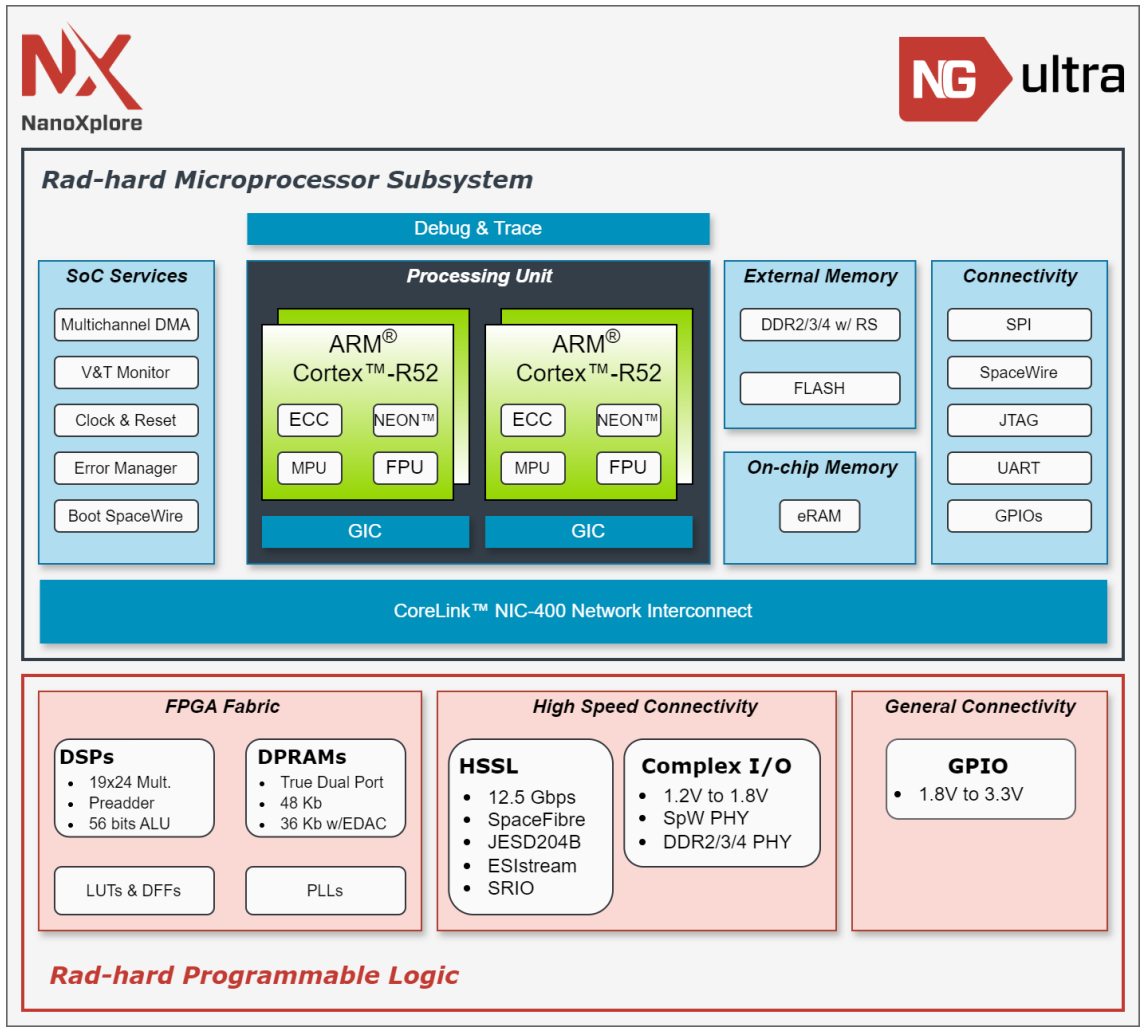
Questions for all of us

Sovereignty	• Could Open Source be an answer to geopolitical instabilities?
Competitiveness	• How to get rid of the technical dept and move forward?
Ecosystem	• How can we stop reinventing the wheel?
Space Specificities	• Are we ready for new challenges?

Who Are We?

- French Based Company : Paris, Montpellier, Grenoble
- 140+ Employees with more than 90% R&D Engineers
- Offer products for Hi-Rel markets
- 3 different products offering:
  - High reliable SoC FPGA
  - ASIC design services
  - Silicon IPs
- ITAR Free Technology
- Focus on Space & Defense markets

What we do?



- **NG-ULTRA**
  - Dual SoC component :
    - Quad Cortex-R52
    - 500K LUTs FPGA Fabric
  - 28nm FDSOI Process
  - SEE Immune
  - Sovereign supply chain
  - First flight models already delivered

- … and other SoC FPGAs & FPGAs with flight heritage

Project – H2020

Design and validation of **U**ltra-**R**eprogrammable s**OC**s

- Specify and design the next generation of ultra-reprogrammable SoC (ULTRA 7) taking benefit of lesson learnt from DAHLIA project
- Validate the SoC on a rad-hard demonstrator in 7nm FinFET technology from TSMC
- Validate reliability and radiation hardening performance of 7nm FinFET
- Introduce SiP concept for space application

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Project Partners

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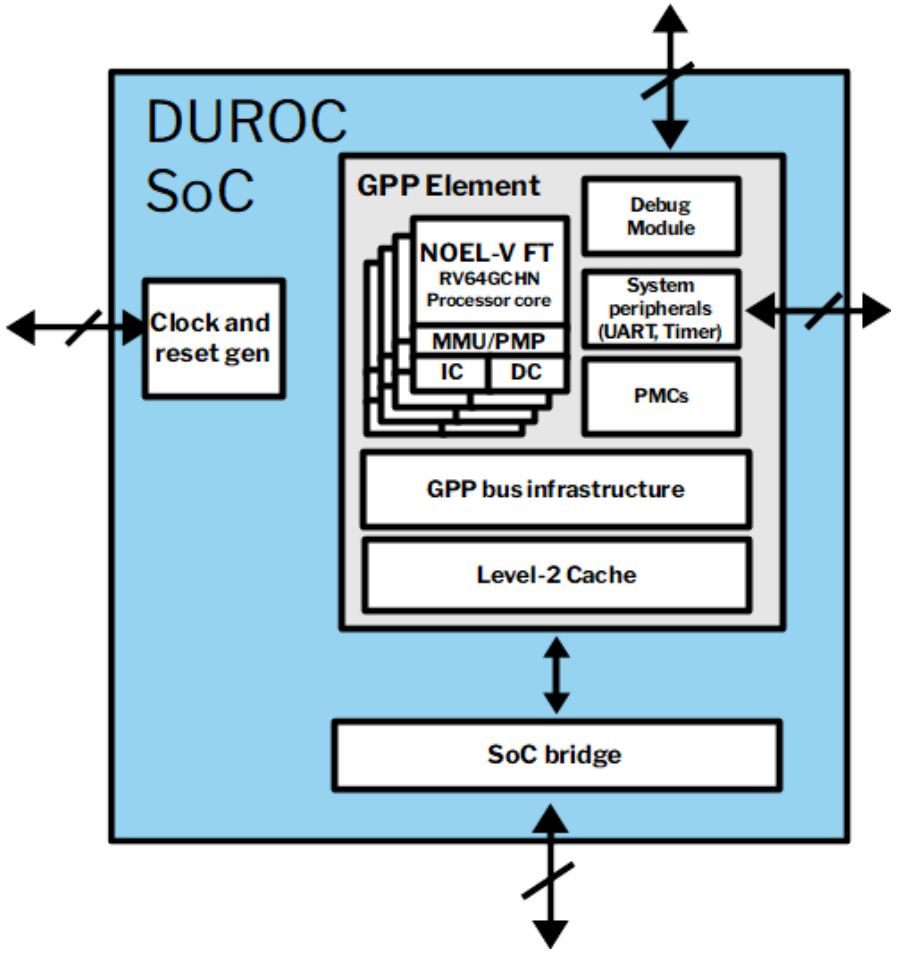
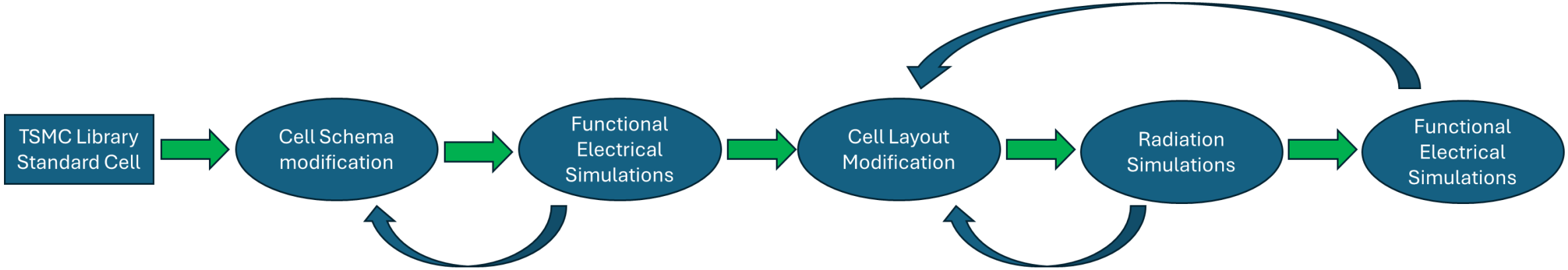
Demonstrator in N7



- Based on Frontgrade Gaisler General Purpose (GPP) element
  - Four 64-bit dual-issue NOEL-V FT RISC-V core
  - Private level-1 cache
  - Shared level-2 cache
- Radiation Constraints
  - TID test up to 150krad
  - Single Event Latchup (SEL): Target LET > 80 MeV.cm²/mg.
  - Single Event Upset (SEU) for FF : target LET > 62 MeV.cm²/mg.
  - Single Event Functional Interrupt (SEFI): target LET > 62 MeV.cm²/mg.
- Thermal Constraints
  - Operational Temperature Range: -40°C to +125°C.
- Samples in Q4 2025

Rad-Hard Standard Cell Development (1)

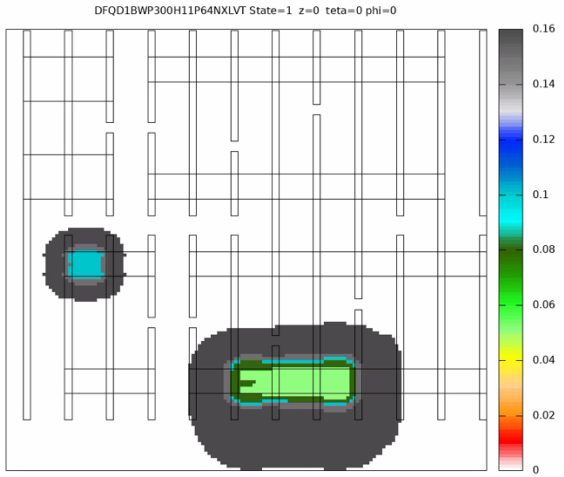
Standard Cell Radiation Hardening flow



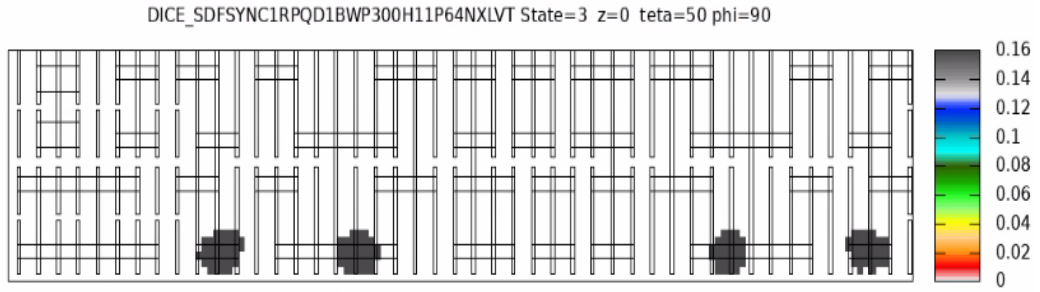
- TSMC foundation standard cells
  - 3 different “flavors” : SLVT, LVT and SVT
  - 2 different families: High Density (HD) and High Speed (HS)
- NX’s first hardening target:
  - LVT (good power vs. performance trade-off)
  - Development with both HD and HS
- Success criteria: Radiation performance as best as we can (target immunity)

Rad-Hard Standard Cell Performance (1)

- Standard and Scan DICE based D-Flop
  - 300l11p64 configuration (300nm row height / Gate length 11nm / Poly pitch 64nm)
  - Radiation performance verification with TFIT.



High-Speed TSMC D Flip-Flop

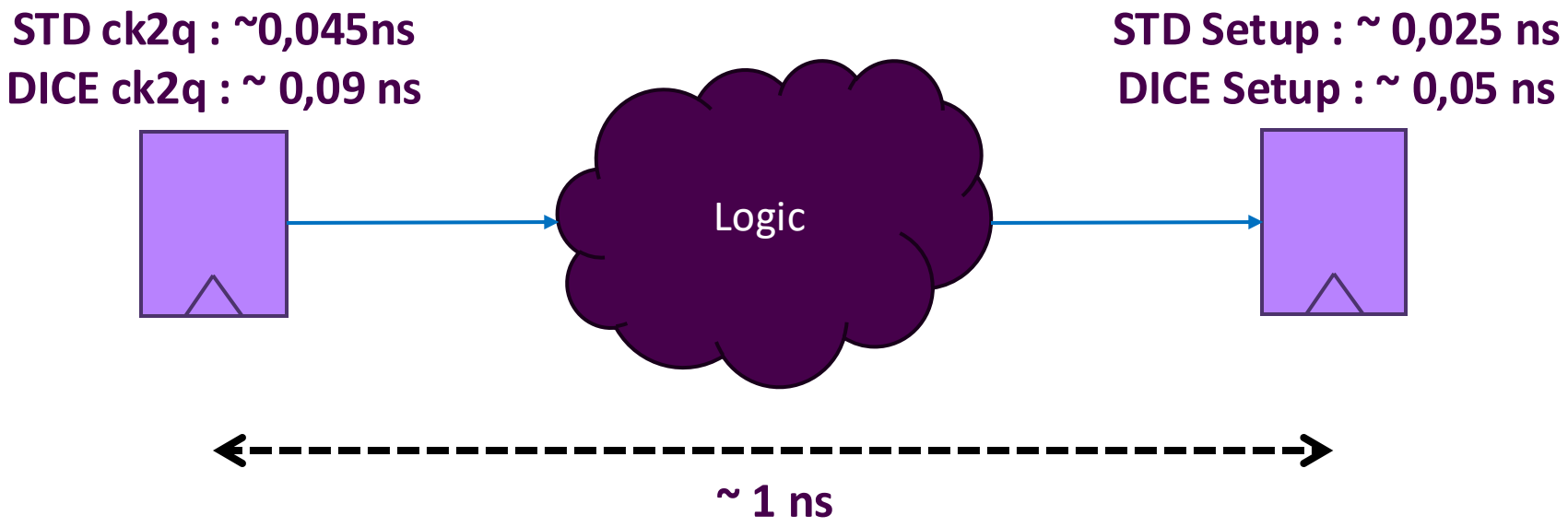


High-Speed NX DICE D Flip-Flop

- DICE DFF vs standard DFF area ratio: 3 – 4 (small silicon contribution)

Rad-Hard Standard Cell Performance (2)

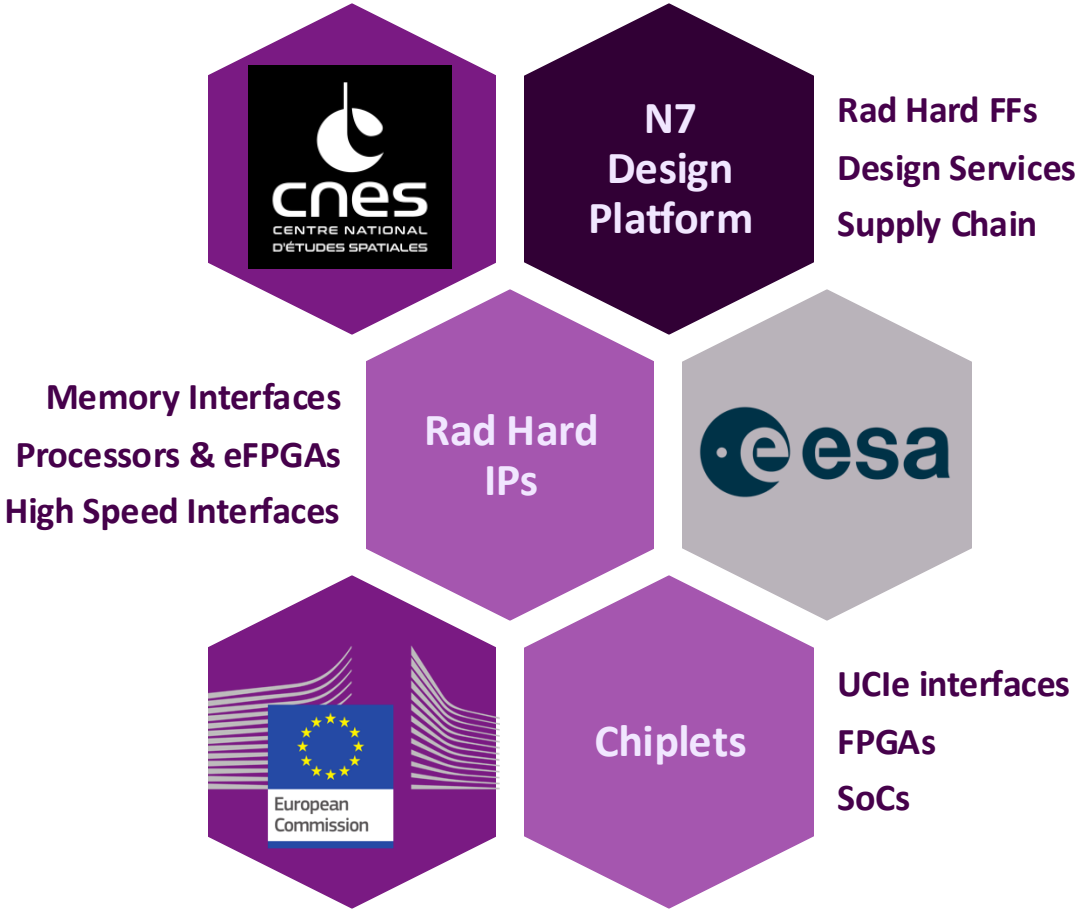
Critical Path Example :

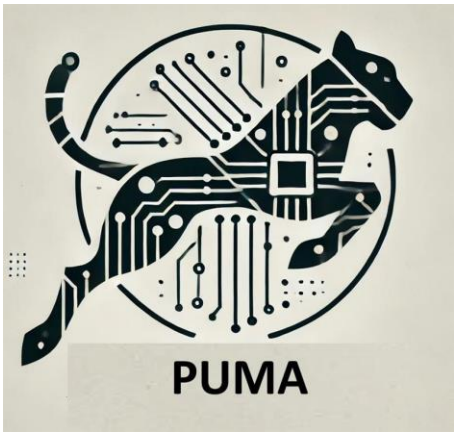


Radiation hardening overhead in a critical path: ~ 6%

What's next?

For the benefit of Ecosystem:
European Space-Ready N7 Design Platform





Thank You

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RISC-V IN SPACE

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