FRONTGRADE Gaisler

GR765 – Octa-Core Rad-Hard Microprocessor

RISC-V in Space Workshop 2025

2025-04-02

Agenda

01 Introduction

02 Processor system

03 Integrated peripherals

04 Authenticated boot and security features

05 Conclusions

FRONTGRADE Gaisler

Introduction

GR765 - Introduction

GR765 is a new processor component for space developed by Frontgrade Gaisler on STMicroelectronics 28nm technology platform.

Successor to GR740 as the high-end processor product in Frontgrade Gaisler's portfolio.

Development supported by European Space Agency ARTES, TDE, GSTP, and NAVISP EL2 programmes, SNSA contract and Frontgrade internal funding.

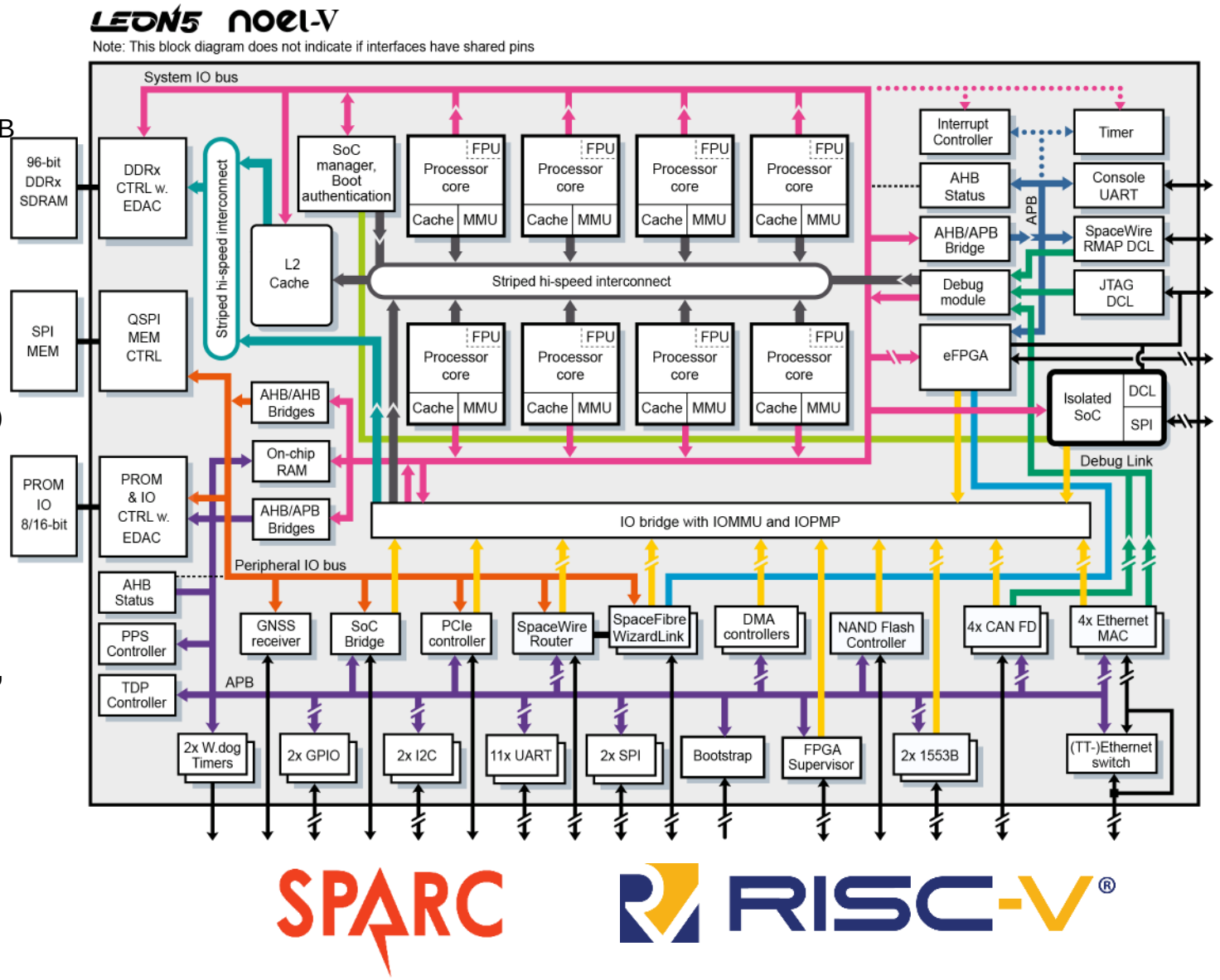
GR765 – Key features

ARCHITECTURE	Octa-core SPARC v8 / RISC-V RV64GCH
QUALIFICATION	ESCC Generic Specification No. 9030
PACKAGE	PBGA 1924 (45x45 mm, 1mm ball pitch)
TID	50 krad(Si) (guaranteed by platform) 100 krad(Si) (testing/screening to be performed)
SEL IMMUNITY	60 MeV*cm^2/mg @125°C
TECHNOLOGY	STM 28nm FDSOI
SUPPLIES	Core: 1.0 V I/O: 1.2 V .. 3.3 V
FREQUENCY	800 MHz, delivering 2600 DMIPS/core
POWER	10 W @ 25°C (TBC)
ORIGIN	Fully developed and manufactured in Europe

SPARC RISC-V®

GR765 – Block diagram

- Fault-tolerant **octa-core** architecture
  - **LEON5FT SPARC V8 or NOEL-V RV64GCH**
  - each core with SIMD extensions, FPU, and MMU, 32 KiB per core L1 cache
  - connected via multi-port interconnect
- 4 MiB L2 cache, **512-bit** cache line, 8-ways
- **DDR2/3/4**
  - 96-bit interface with dual x8 device correction capability
  - 80-bit interface with x8 device correction capability
  - 72-bit interface with error detection capability (SECDED)
- 8/16-bit PROM/IO interface
- **(Q)SPI and NAND memory controller interfaces**
- **eFPGA 30k LUT**
- **Built-in GNSS receiver for (GPS and Galileo)**
- **Hardware authenticated boot (hybrid scheme with ECDSA, ML-DSA)**
- **Isolated SoC / HSM for HW RoT, Secure Boot, Crypto**
- **DMA controllers**



SPARC RISC-V®

GR765 – Raw numbers comparison with GR740

Metric	GR740	GR765	Change
CPU performance	4-core, single-issue, 250MHz	8-core, dual-issue, 800 MHz	12X
RAM capacity	SDRAM PC100, 512 MiB	DDR4-1600, 16 GiB	32X
RAM bandwidth	64 x 100Mbps = 6.4 Gbps	64 x 1600 Mbps = 100 Gbps	16X
IO bandwidth (in+out)	PCI 32x33M = 1Gbps SpW 8x2x200M = 3.2 Gbps	PCIe 8x2x4G = 64 Gbps SpFi 4x2x6.25 = 50 Gbps	27X

FRONTGRADE Gaisler

Processor system

NOEL-V – RISC-V Processor

- **RISC-V processor core**
- Superscalar – in order pipeline
- RV64GCH – 64-bit processor
  - 64 Base integer instructions (I)
  - MUL/DIV (M)
  - Atomics (A)
  - Half/Single/Double Precision Float (Zfhmin, FD)
  - Compressed instructions (C)
  - Hypervisor (H)
  - Bit manipulation (subset of) (B)
  - Physical Memory Protection (PMP)
  - MMU - 39 bit virtual addressing, separate I and D, fully associative, TLB
- Cache control extensions
  - Cacheline invalidate, zero, etc (Zicbom, Zicbop, Zicboz)
  - Cachability in page tables (Svpbmt)
- RISC-V Advanced Interrupt Architecture (AIA)

Performance:

- Comparable to ARM Cortex A53
- CoreMark*/MHz: 5.02**

* gcc (ge0886d8ad) 15.0.1 20250330 (experimental)
-O3 -ffast-math -march=rv64imafdc_zba_zbb_zbc_zbs_zbkb_zbkc_zbkx_zicond_zifencei_zfh_zicbom -mabi=lp64d -finline-functions --param max-inline-insns-auto=20 --param inline-min-speedup=10 -funswitch-loops -funroll-all-loops -fgcse-after-reload -fpredictive-commoning -fipa-cp-clone -falign-jumps=8 -falign-functions=8 --param=l1-cache-line-size=32 --param=l1-cache-size=16

** Using "#define ee_u32 int32_t" in core_portme.h, as is common for 64 bit RISC-V.

Instruction Set Architectures

Why RISC-V?

- Hardware and software potential for future space applications: A new class of processors requires a modern architecture
- Enabling new technologies by standardization
  - Hypervisor support
  - Vector extension, …
- Growing base of 3rd party ecosystem:
  - Toolsets
  - Libraries, engines etc.
- Attractive to talent entering the space domain
- Influx of know-how by talent entering the space domain

Why SPARC?

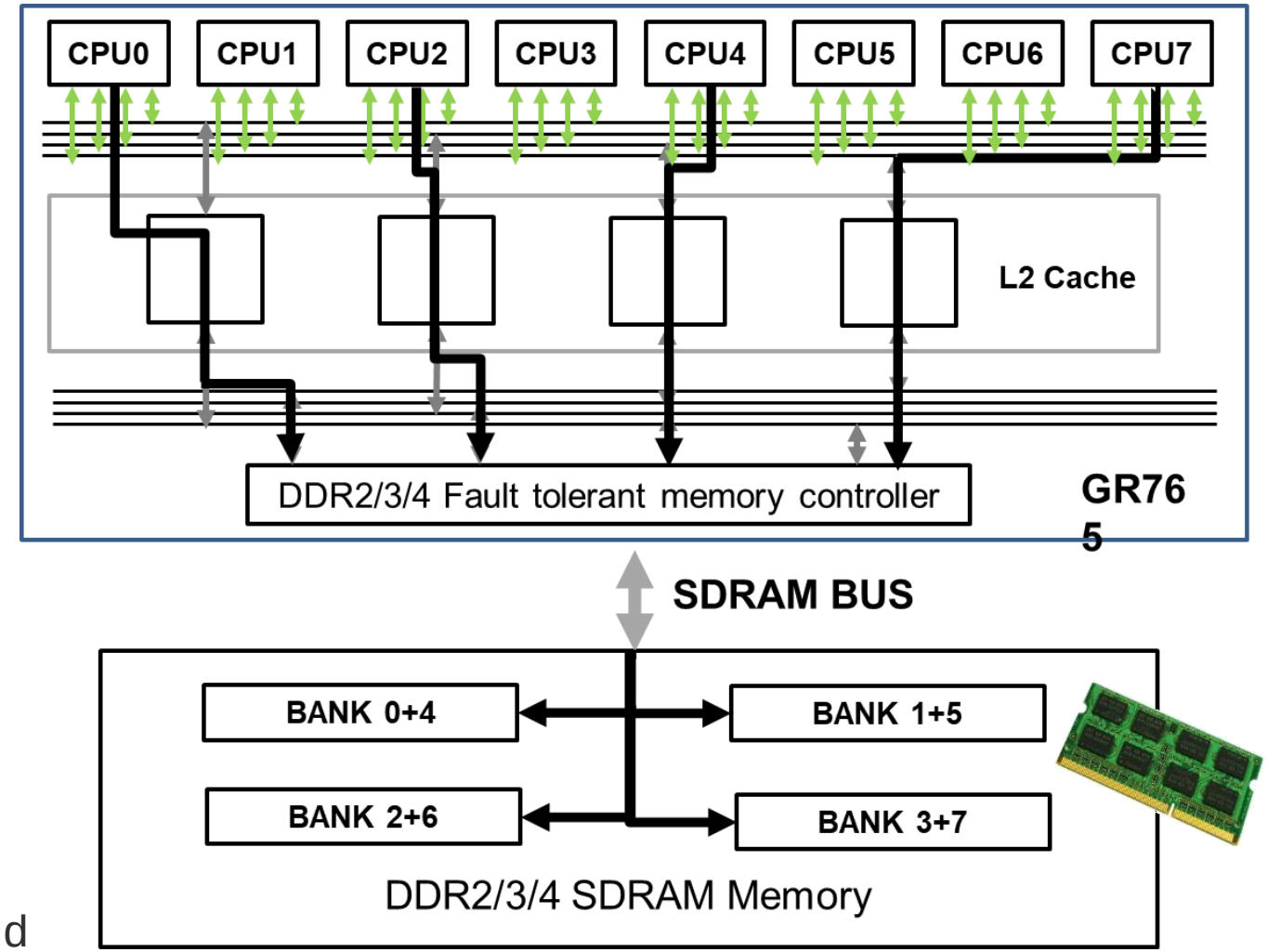
- Existing base of space proven HW and SW designs
- Mature ecosystem for today's space applications, e.g. qualified OS
- Accumulated development know-how in the industry
- Software backward compatible with existing LEON devices

GR765 provides RISC-V and SPARC

- Both architectures are needed by the industry
- Faster time-to-market for RISC-V while continuing SPARC – ease transition between the two architectures
- Minimal silicon overhead - sharing of resources on chip. User selects CPU (LEON5FT or NOEL-VFT), device cannot operate with both at the same time.

GR765 – Improved interconnect

- Banked / Striped on-chip bus interconnect creating four separate L2+bus hierarchies that map to different internal banks of the SDRAM.
- CPUs accessing two different stripes will have zero interference on L2 hit and near-zero on L2 miss.
- Mapping between linear RAM address (as seen from software/DMA) and stripes reconfigurable. Can be tuned for performance/scaling, timing isolation or hybrid of the two.
- This striping approach is fully cache-coherent and transparent to software.



FRONTGRADE Gaisler

Integrated peripherals

GR765 – Peripherals overview

- High speed interfaces:
  - SpaceFibre, 6.25 Gbps, 4 links
  - PCI-express gen 3 (4 Gbps), 8 links (1x8 or 2x4 configuration)
- Industry standard interfaces:
  - SpaceWire
  - CAN / CAN-FD
  - Gigabit Ethernet (RGMII)
  - MIL-STD-1553B
  - I2C, SPI, UART

- In addition, the GR765 has many integrated functions to reduce the need for companion FPGAs:
  - NAND flash controller
  - Embedded 32kLUT FPGA
  - Time-Triggered Ethernet Switch
  - GNSS Receiver IP
  - Spacewire router with Spacewire-to-SpaceFibre bridging capability
  - External FPGA scrubber

GR765 – embedded FPGA

- **GR765** will incorporate a **NanoXplore eFPGA**

- **32k LUTs + 40x 48kbit BRAMs**

- The eFPGA subsystem will be possible to operate **without processor** intervention.
- **Reprogramming** of the eFPGA will **not affect processor execution**.
- The eFPGA subsystem will be **programmable** from **processors**.
- AMBA AHB and APB ports will be **accessible** to **processor subsystem**.

- **Bitstream authentication** will be available.

- Supported by **standard NanoXplore tool set.**
- Supported by **GRLIB IP** cores.

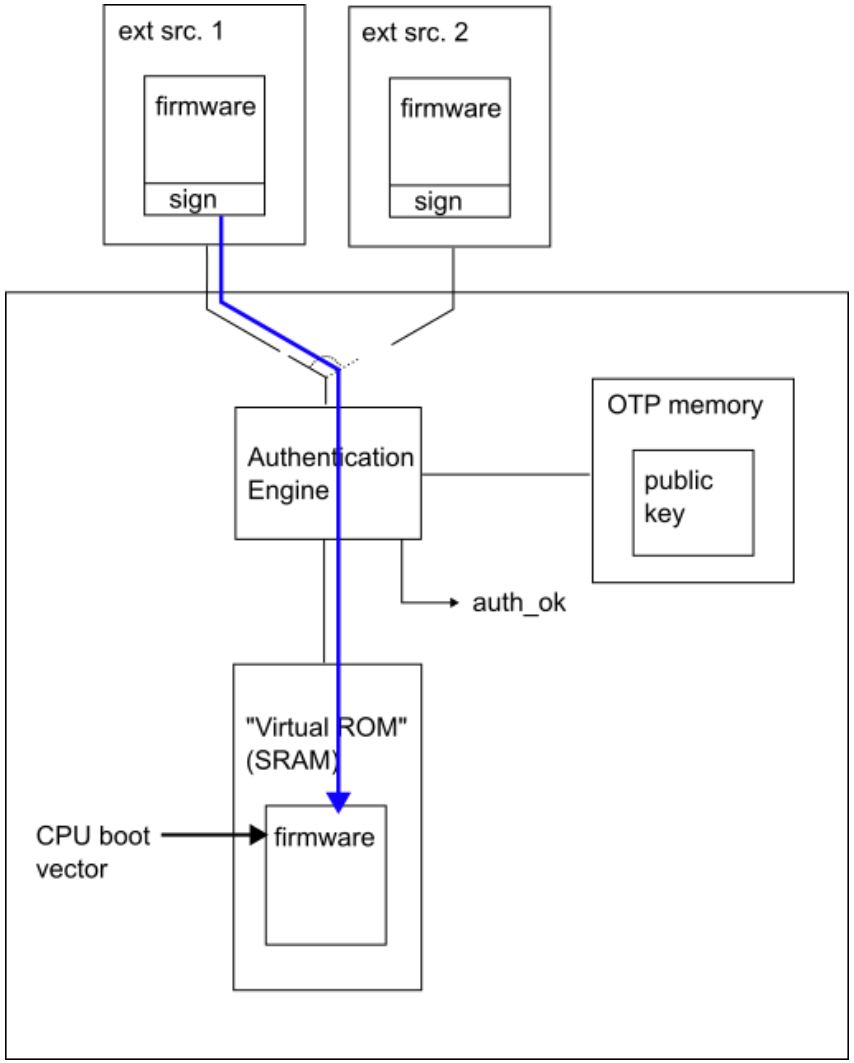
NanoXplore

FRONTGRADE Gaisler

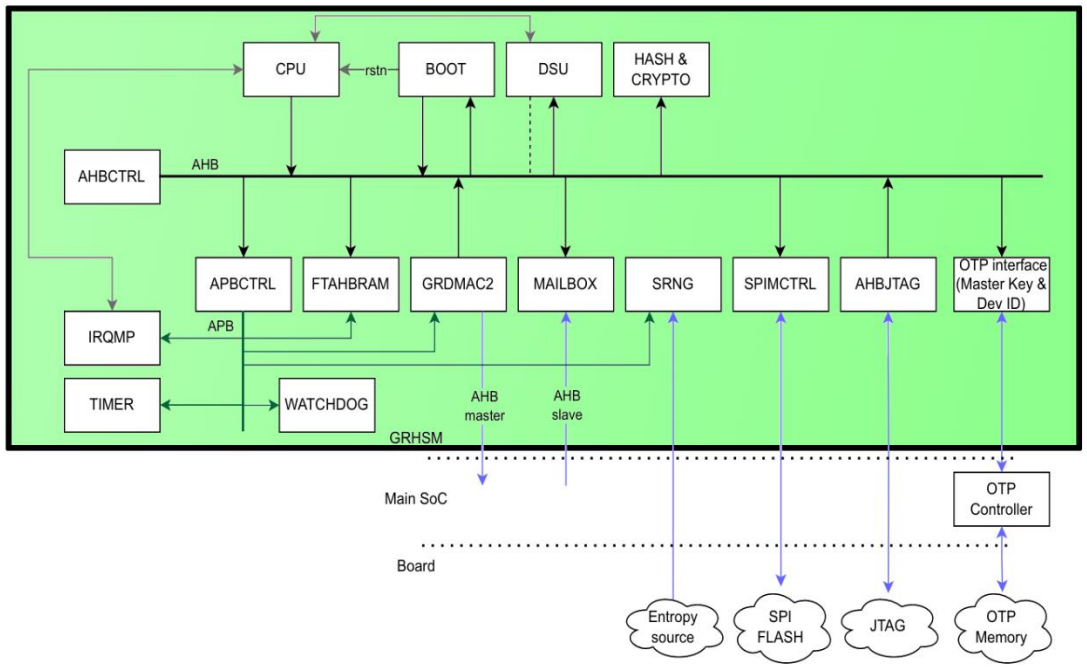
Authenticated boot and security features

GR765 – Authenticated boot scheme

- Scheme to extract first stage of software into on chip memory and verify cryptographic signature before CPU starts running
  - With retry from alternate sources
- Using hybrid classic+PQC public-key signature verification algorithm implemented in hardware with public key stored on-chip in one-time programmable memory (OTP).
- Software-free process, managed by central SoC boot manager state machine and using hardware crypto accelerator cores.



GR765 – Isolated Subsystem / Hardware Security Module



- Intended usage is as a hardware security module to perform attestation, key generation and other security/crypto-related tasks.
- Cores for SHA256 acceleration, and entropy/randomness generators for key generation.
- Working with third party provider to develop off-the-shelf software offering for the Isolated Subsystem
- Separate SoC with private external SPI flash storage that interfaces the rest of the system via a mailbox interface. Independent execution after device reset.
- Not mandatory for using the rest of the device, for applications that do not require this type of functionality.

FRONTGRADE Gaisler

Software support

Next-Generation SoC

Software

- Complete ecosystem
- A combination of Gaisler and 3rd party software

Tool chains, Operating systems and compilers

- Bare-C
- Linux
- RTEMS
- VxWorks
- Zephyr

Hypervisors

- XtratuM/XNG (FentISS)
- PikeOS (SYSGO)
- Xvisor

Boot loaders

- MKPROM2
- GRBOOT Flight bootloader

Tools

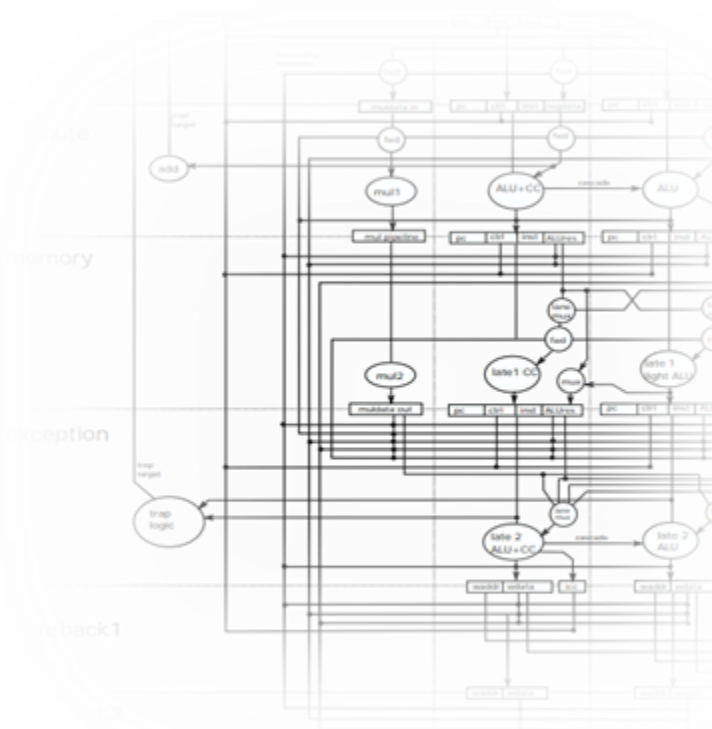
- GRMON3
- TSIM3

FRONTGRADE Gaisler

Conclusions

GR765 Conclusion

- The GR765 development builds on the successful GR740 quad-core LEON4FT component, with a major leap in performance and numerous additional enhancements.
- The GR765 is an **octa-core** processor. Users can enable either eight NOEL-VFT RISC-V 64-bit processor cores or eight LEON5FT cores.
- GR765 supports DDR2/3/4 SDRAM, high-speed serial link controllers and several other extensions.
- The GR765 development puts emphasis on computational performance, power efficiency, and support for mixed criticality application with a high degree of integration to allow an overall cost, space and power efficient board-level solution.
- The GR765 is supported by a strong software ecosystem.

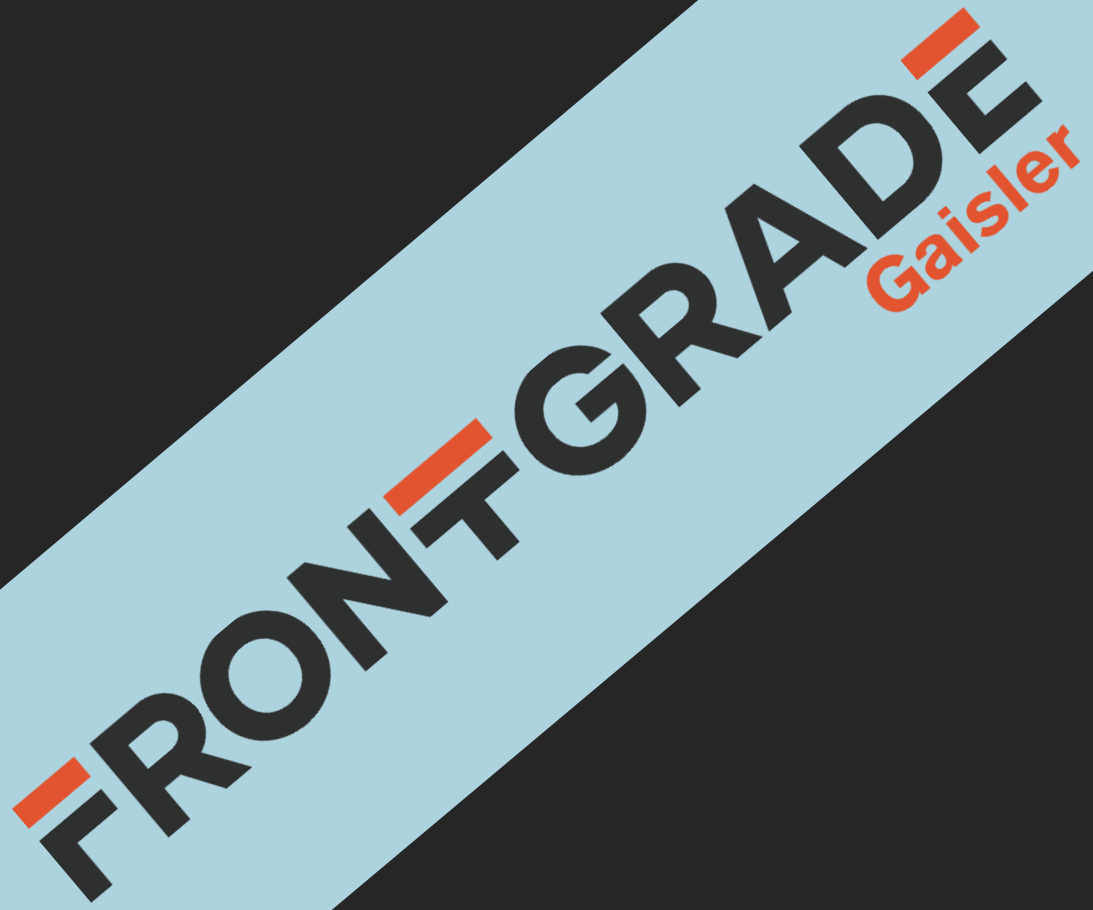


noel-V LEON5

FRONTGRADE Gaisler

Thank you for listening!

https://www.gaisler.com/products/gr765


FRONTGRADE
Gaisler