EuroHPC
Joint Undertaking

RISC-V and EuroHPC : Powering Europe's Future in High-Performance Computing

RISC-V for Space Workshop

3rd April 2025 | **Alexandra Kourfali** | Gothenburg, SW

Who are we?

- EU body & legal and funding entity
- Created in 2018
- Autonomous since Sep. 2020
- Based in Luxembourg
- A team of 45+ employees
- Still growing!

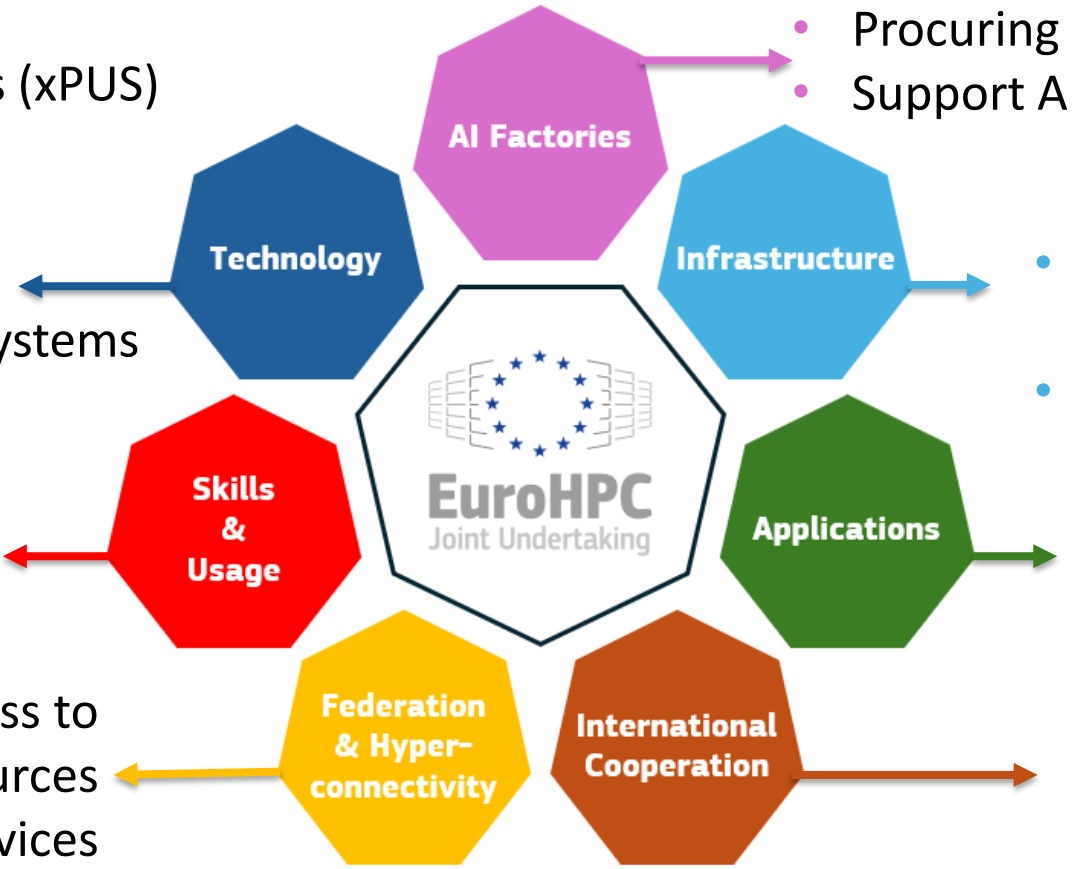
Our Mission

R&I activities to develop:

- **Hardware** components (xPUS)
- **Pilots**
- **Software** stack
- **Quantum** integration
- **Energy-efficient** HPC systems

- **Training** programmes to develop HPC skills base in Europe

- Development of access to **federated** HPC resources and services



- Procuring /upgrading **AI**-oriented HPC **systems**
- Support AI app development in EU

- **Procuring**/deploying HPC & QC SOTA systems
- Providing **access** to EU users

- Algorithms, SW development
- **Centers of Excellence**

Collaboration with **3rd countries**

- Solve global challenges
- Strengthen EU competitiveness

EuroHPC Supercomputers

Procured

3 PRE-EXASCALE

- Lumi, FI #5 TOP500
- Leonardo, IT #7
- Marenostrum 5, ES #8

5 PETASCALE

- Vega, SL
- Karolina, CZ
- Discoverer, BG
- Meluxina, LU
- Deucalion, PT

Ongoing

2 EXASCALE

- Jupiter, DE #1 Green500
- Alice Recoque, FR

2 MID-RANGE

- Arrhenius, SW
- Daedalus, GR

Coming Up Next

UPGRADES

- Discoverer+
- Lisa/Leonardo

AN INDUSTRIAL SYSTEM

- Use by the industrial sector
- AI focused

A POST-EXASCALE SYSTEM

PROCUREMENT OF FEDERATION SERVICES

EuroHPC Quantum computers

Selected

Quantum Computers

- EuroQCS-Poland
- Euro-Q-Exa, DE
- EuroQCS-France
- LUMI-Q, in CZ
- EuroQCS-SPAIN
- EuroQCS-ITALY

Upcoming:

- MeluXina-Q, LU
- Quantum in NL

Consortia of 30+ countries

Quantum Simulators

deployed, to be integrated in:

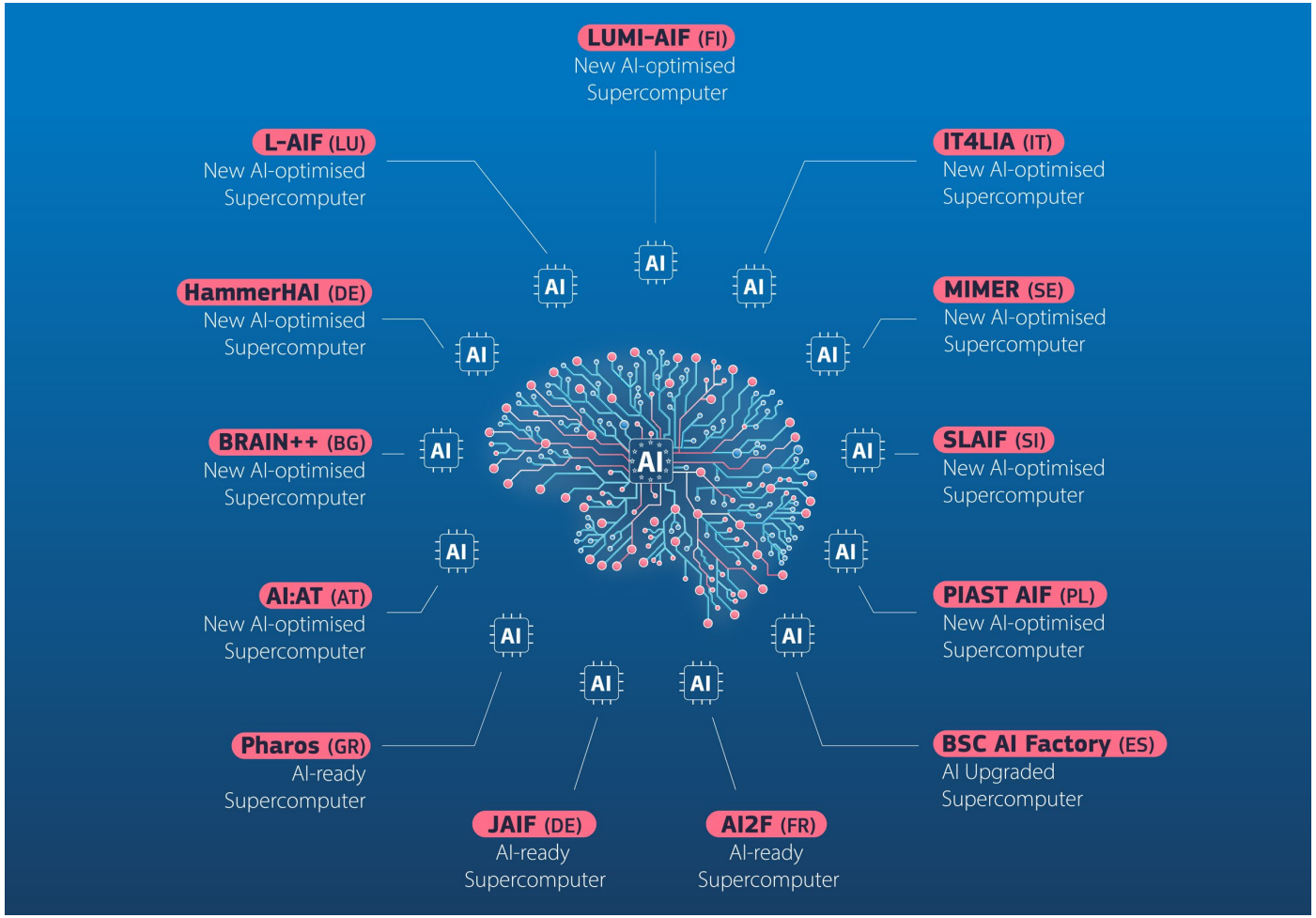
- Joliot Curie, in France
- JUWELS, in Germany

Coming Up Next

- Finalising procurements
- Development of HPC-QC middleware technologies
- Quantum Excellence Centres
- Scientific collaboration on quantum with 3rd countries
- First system expected to be operational in 2025

EuroHPC AI factories

EuroHPC JU selected 13 EU sites that will host the first AI Factories – to drive Europe's leadership in AI



AI-ready EuroHPC supercomputers in:

- Germany **JAIF** – JUPITER
- France **AI2F** – Alice Recoque
- Greece **Pharos** – Daedalus

AI-upgrades to EuroHPC supercomputers in:

- Spain **BSC AIF** – MareNostrum 5

New AI-optimized EuroHPC supercomputers in:

- Finland **LUMI-AIF**
- Germany **HammerHAI**
- Italy **IT4ALIA**
- Luxembourg **L-AIF**
- Sweden **MIMER**
- Bulgaria **BRAIN++**
- Slovenia **SLAIF**
- Austria **AI:AT**
- Poland **PIAST AIF**

*AI Factories pull together EU and national resources, in a collaborative effort of **21 European countries***

Our Organization

Co-funded by EU, Participating States and Private Members

The European Union
represented by the
European Commission

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3 Private Members

34 Participating States

Our Organization

Co-funded by EU, Participating States and Private Members

European Commission

Digital Europe
1.98 B€
- Infrastructure
- HPC services Federation
- Usage, skills

Horizon Europe
900 M€
- **Technology**
- Applications
- International Cooperation

Connecting Europe
200 M€
- Hyperconnectivity
- Data connectivity

Total investments
7 B€ in 2021-2027

R&I
≈ 2 B€ in 2021-2027

900 M€
from 3 Private Members

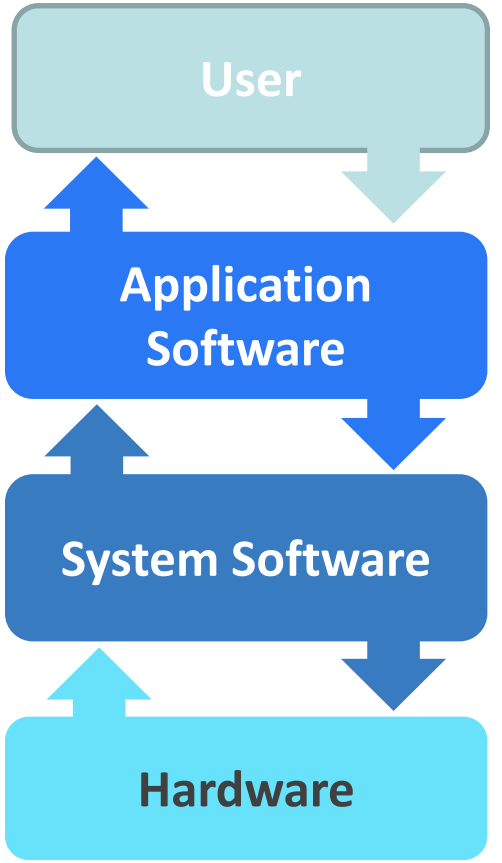
3 B€ from
34 Participating States

Currently around **40 R&I projects** on **technology, applications & skills**

Strategic Research & Innovation areas

EuroHPC JU funds an R&I programme to develop a full **European supercomputing ecosystem,** support European **digital autonomy,** to reduce Europe's dependency on **foreign manufacturers**

- **Leadership in Use & Skills**
  Competence Centres & training programmes in HPC commensurate with the labour market.
- **Applications and Algorithms**
  Centres of Excellence for HPC Applications & algorithms for EU exascale
- **European Software Stack**
  SW, algorithms, programming models and tools for exascale & post exascale
- **European Hardware**
  Ecosystem for low power high-end general purpose processor & accelerator



Microprocessor technology: Strategy

EU goal: autonomy in strategic processing technologies

*Our **ambition:** by 2030*

- *The production of cutting-edge and sustainable semiconductors in Europe including processors is at least **20% of world production** in value*
- *Manufacturing capacities below **5nm** nodes aiming at 2nm*
- ***Energy efficiency** 10X more than today*

✓ ***RISC-V ISA plays a central role on EU's technology strategy***

✓ ***AI needs are reforming EU's strategy in processors***

HPC microprocessor technology: Strategy

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EU goal: autonomy in strategic processing technologies

DESIGN

Short term (2025-27)

First IPs

- **Build on EPI** efforts
- From test chips to **TRL 9**
- RISC-V processors and accelerators: chiplets, advanced nodes
- EuroHPC exascale systems as first customer and scale to **embedded**

Medium term (2028-30)

New RISC-V architectures complement the work of EPI and DARE

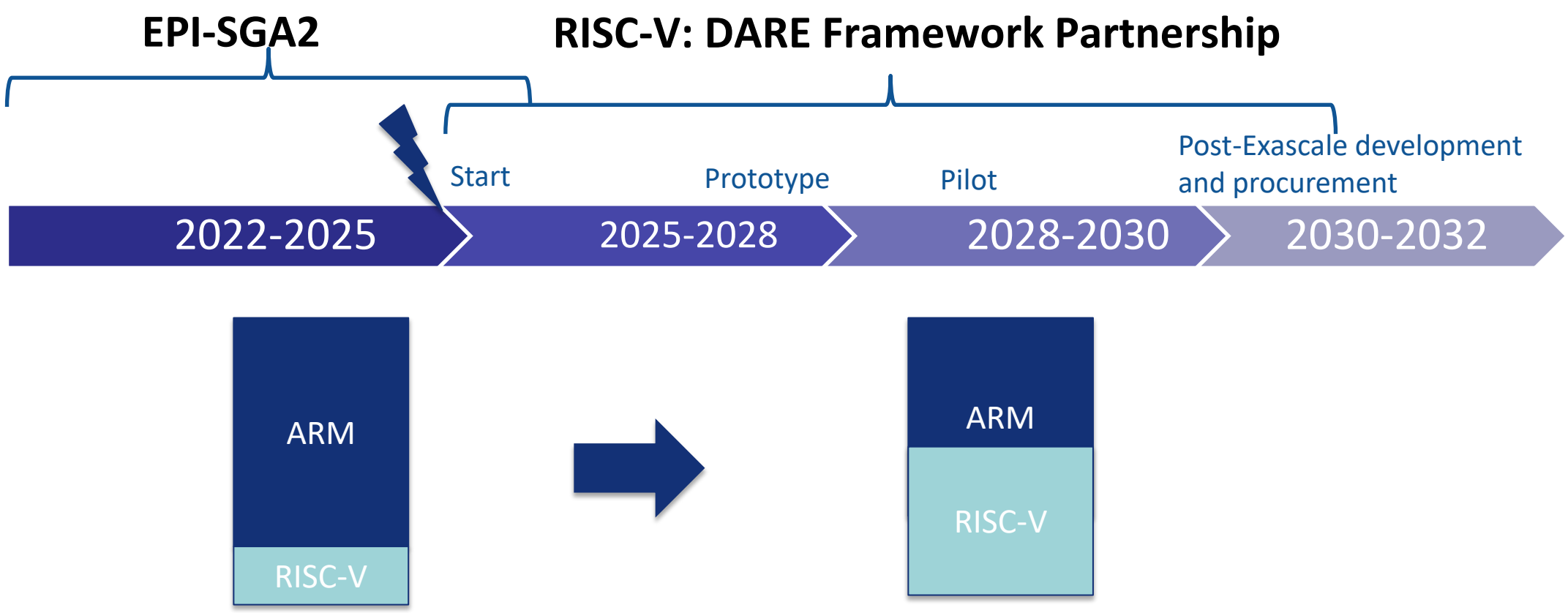
- Pilots on RISC-V with stand-alone competitive xPUs
- Collective effort building on **EU R&D** in low power, AI, security,…,
- EuroHPC **post-exascale** system as first customer

Long term (2030-)

Post-exascale RISC-V systems based on EU R&D

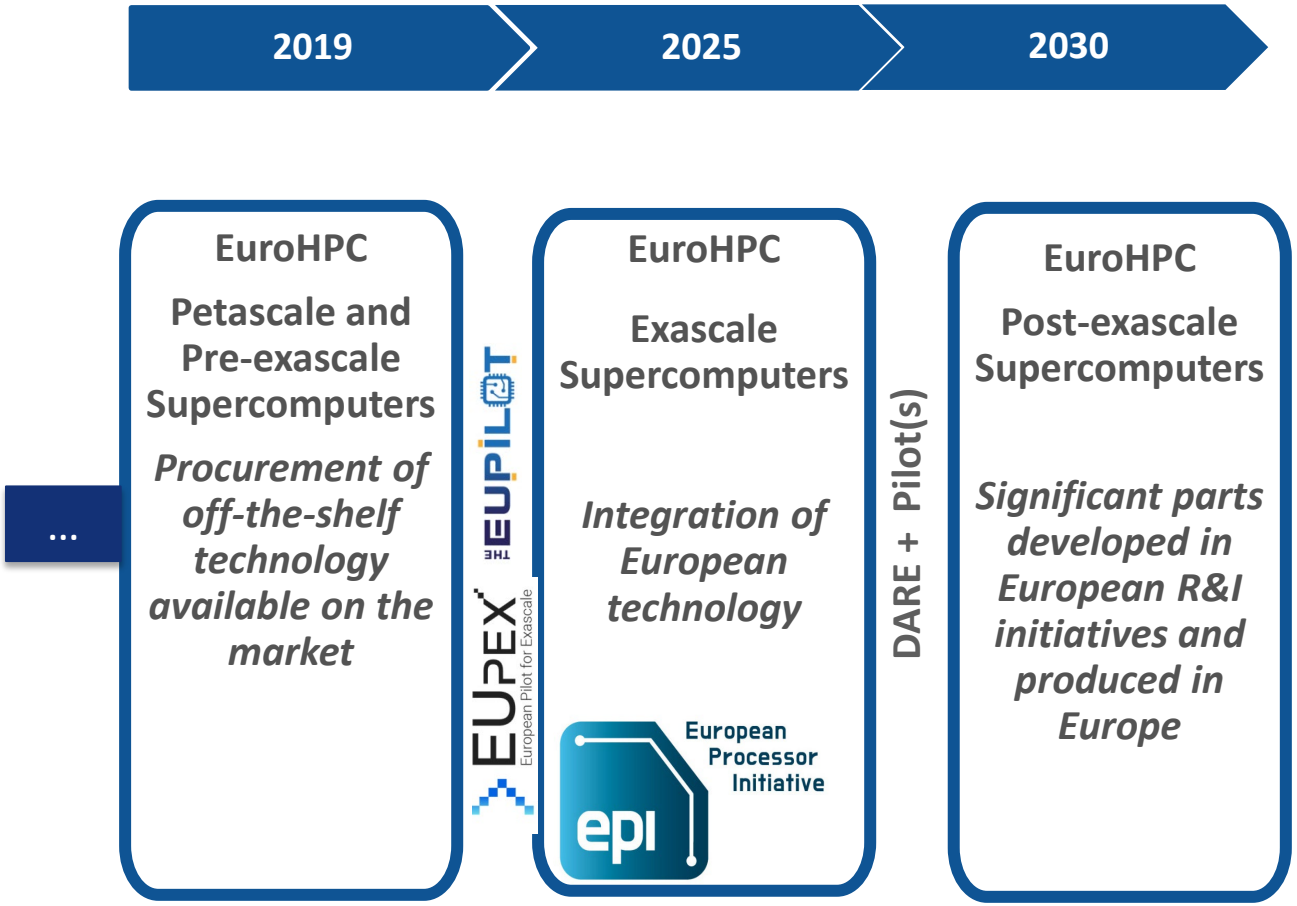
HPC microprocessor technology

State of play



Ongoing EU activities on HPC Technology

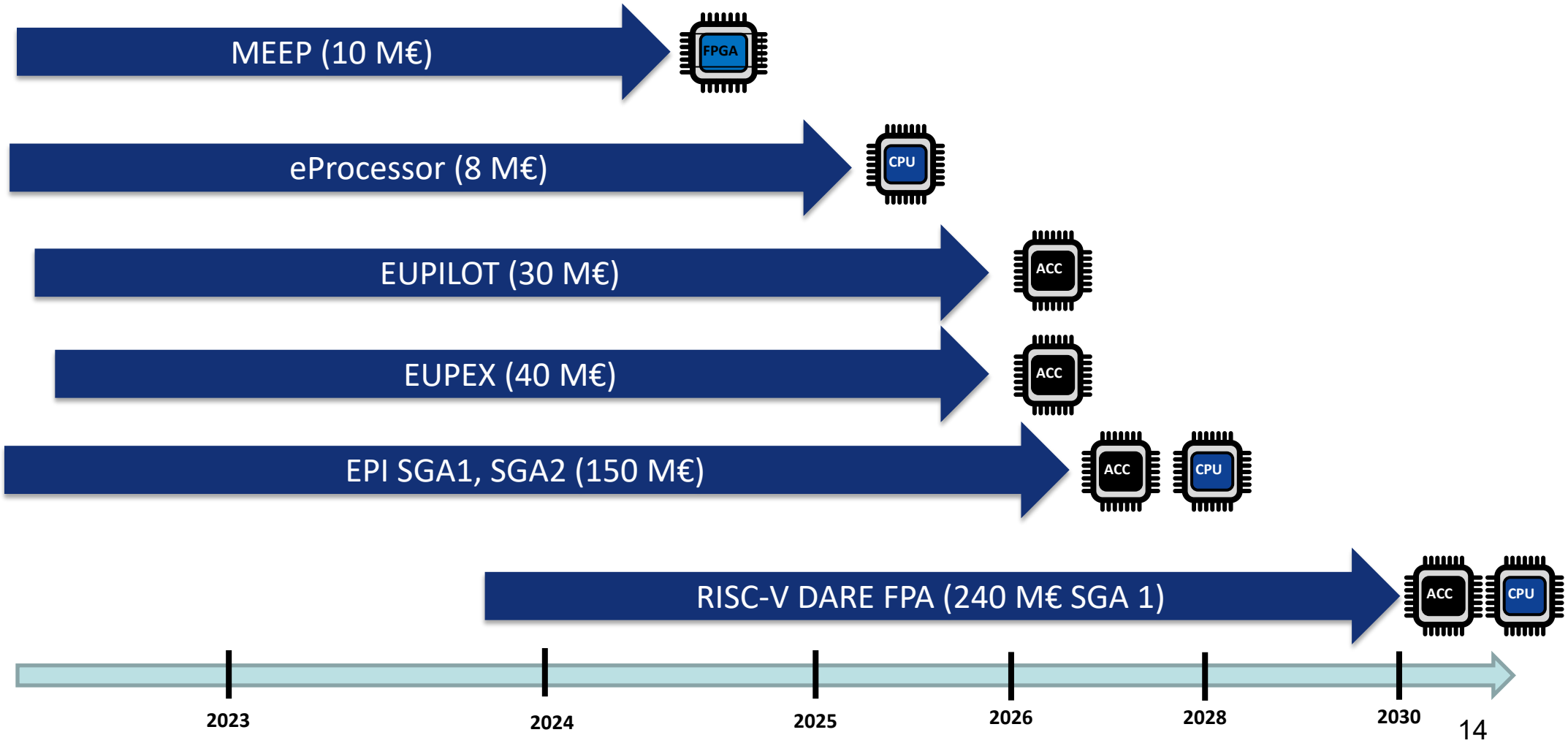
EU goal: autonomy in strategic processing technologies



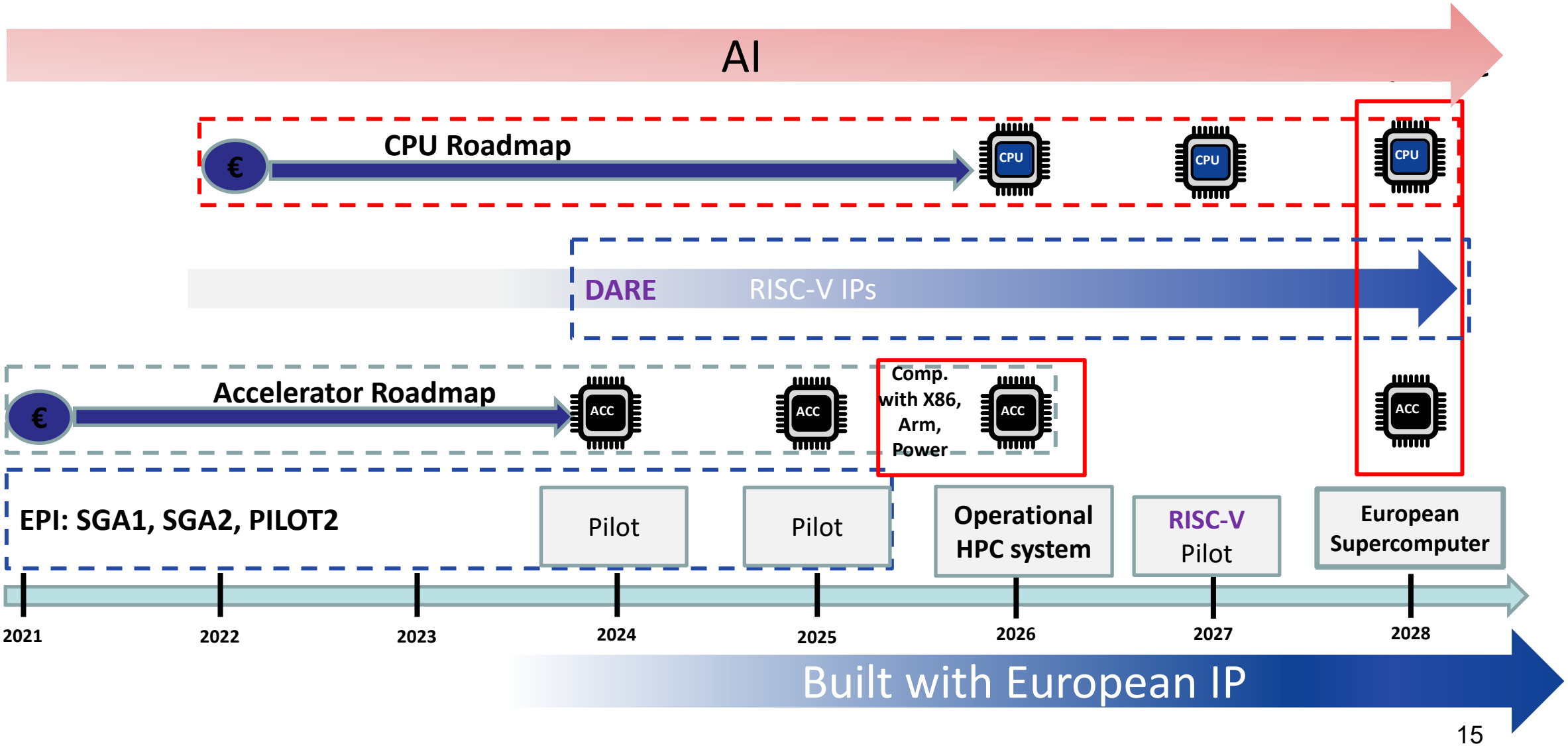
- **Strategic R&I roadmap** to design and deliver energy efficient **open hardware technology**
- **Framework Partnership** Agreements:
  - **EPI:** European low-power microprocessor technologies
  - **DARE:** Large-scale European initiative for High Performance Computing ecosystem based on RISC-V

EuroHPC state of play in HW design

xPUs for HPC

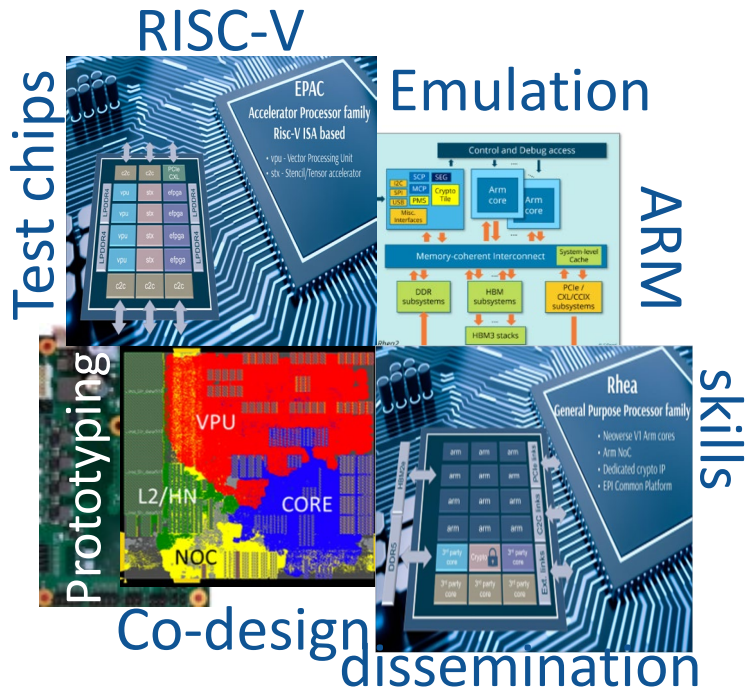


EuroHPC Chips Roadmap



EPI-SGA2 at EuroHPC

EPI umbrella and ecosystem



EPI-SGA2 at EuroHPC

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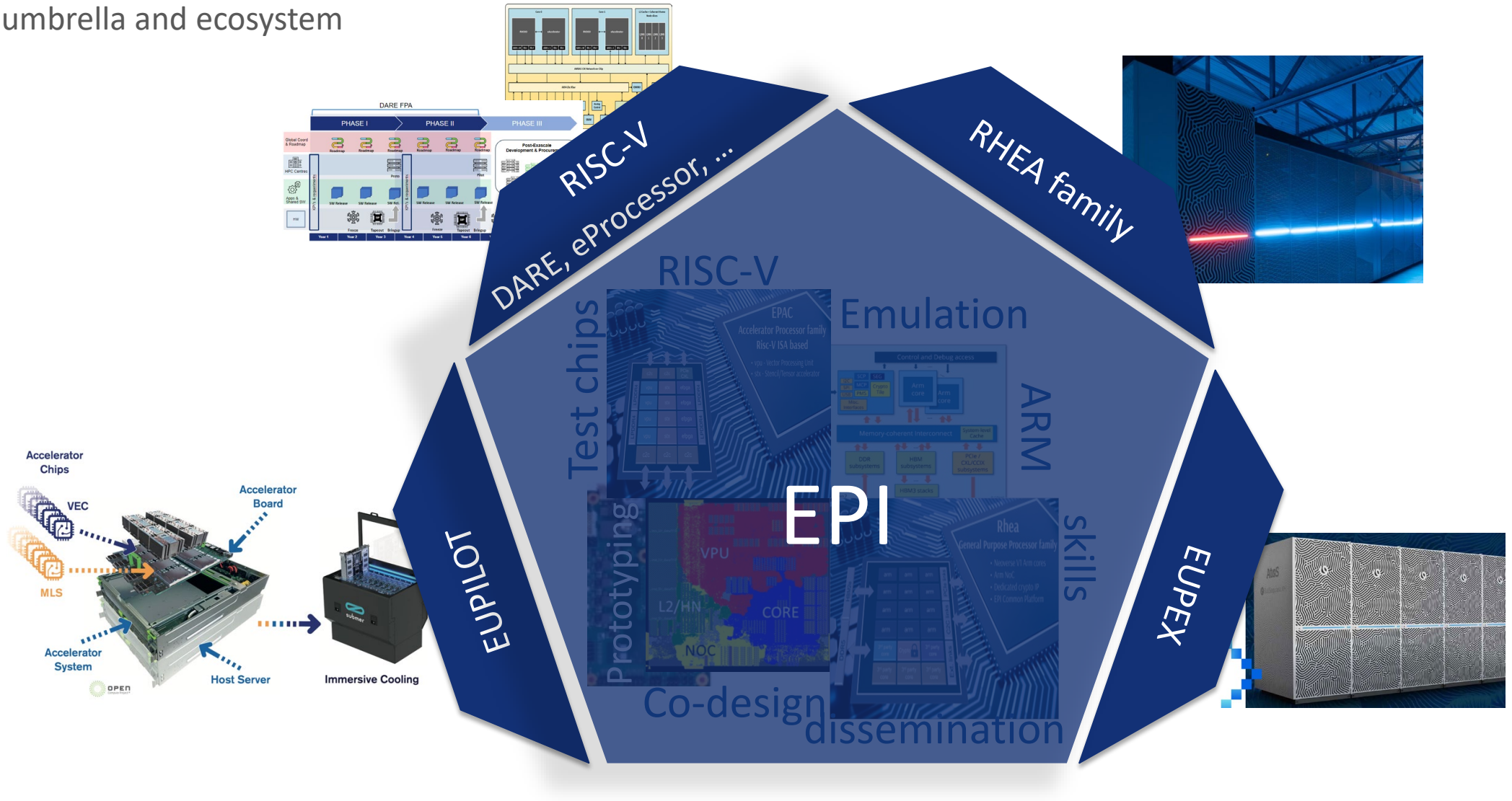
EPI umbrella and ecosystem

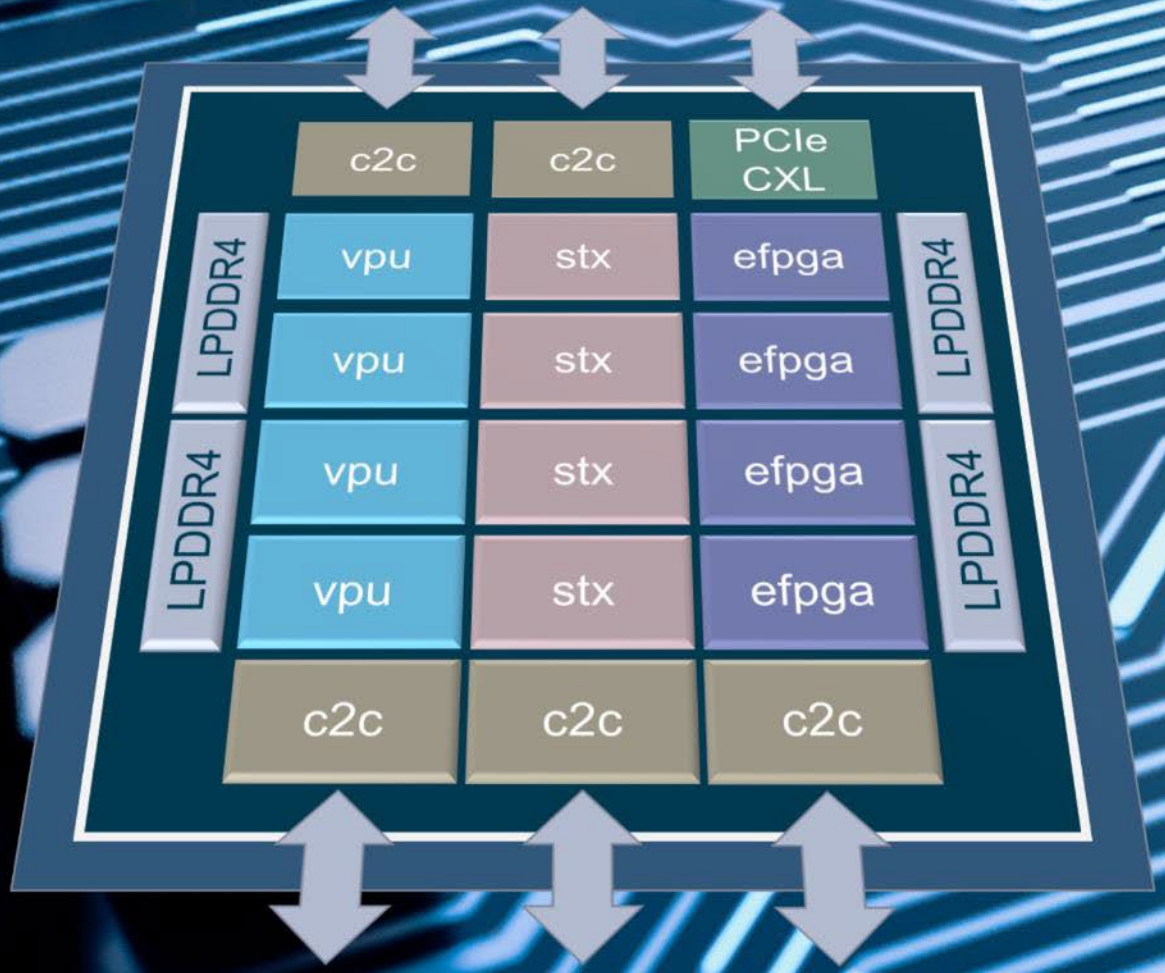


EPAC

Accelerator Processor family

Risc-V ISA based

- vpu - Vector Processing Unit
- stx - Stencil/Tensor accelerator



EPI Co-design and Validation

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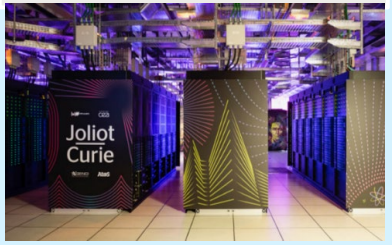
Hardware platforms

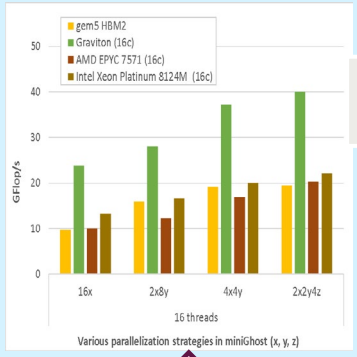
Refer. Platforms



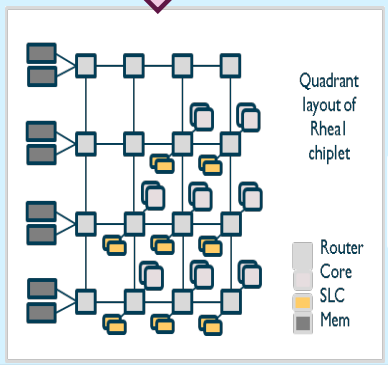
SDVs

EPI Prototype

Validation and Co-design



Validation



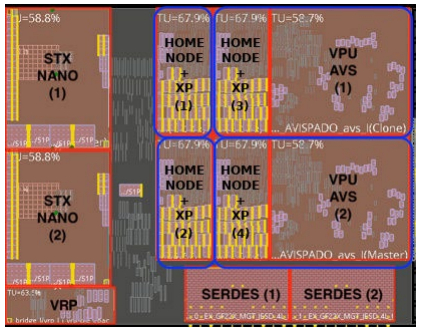
Codesign

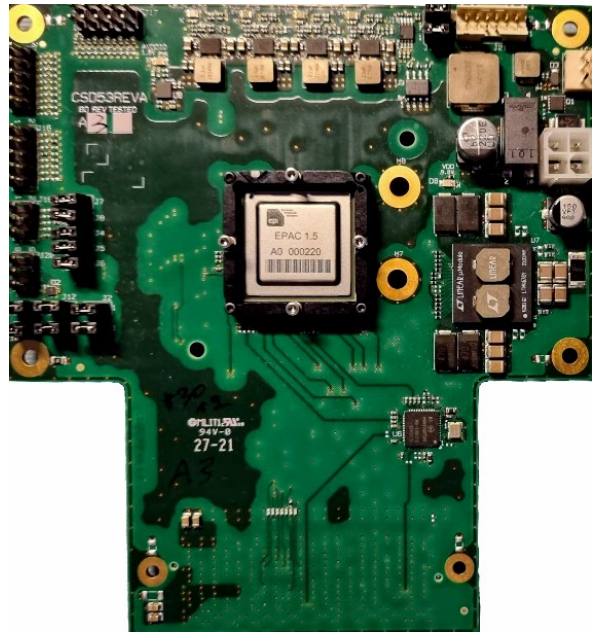
EPI architects

Future Chips

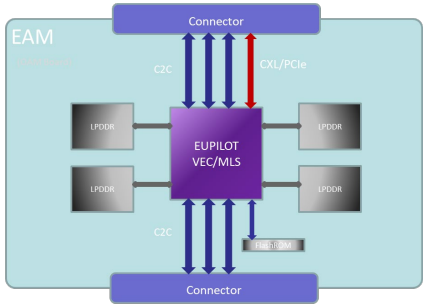
RISC-V chips development status

EPI
- EPAC 1.5 (2nd gen)
- SDV



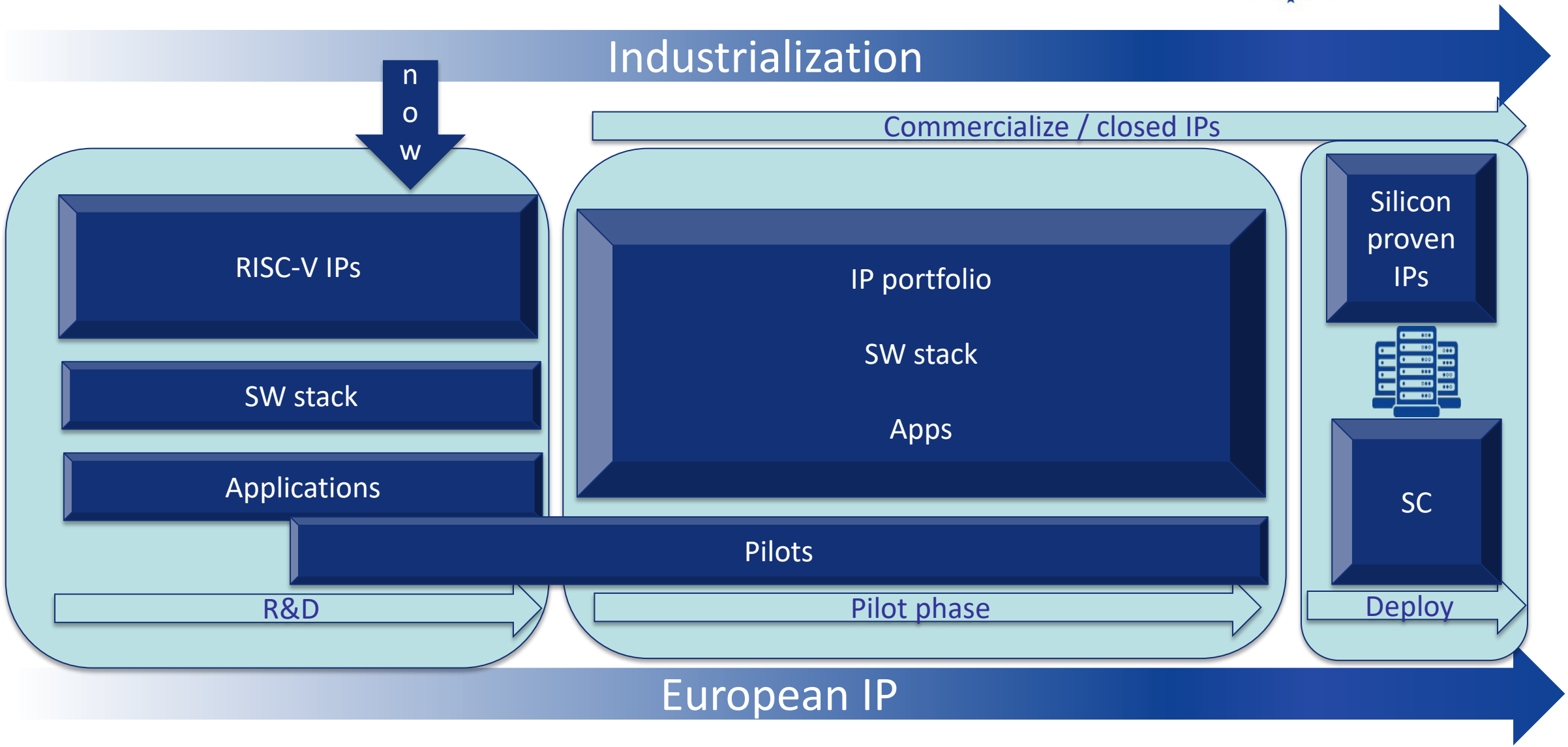


EUPILOT
- VEC: Global Foundries 22 nm
- Next GEN:
  - VEC : 59 mm² GF 12nm
  - MLS : 20 mm² TSMC 7nm

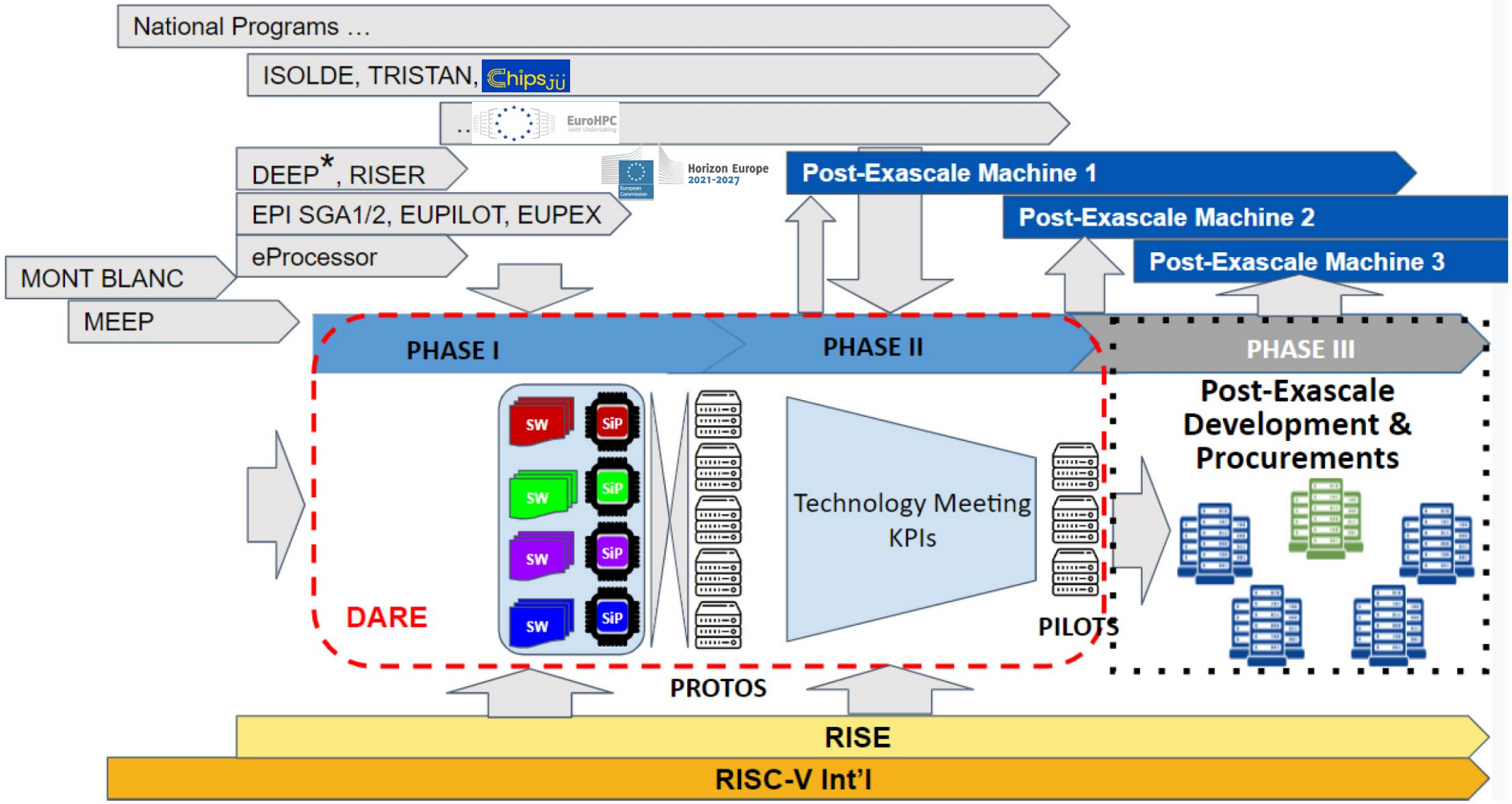


eProcessor
- 1 RVOOO core, 1 eAccelerator, 2 L2 slices
- GF 22nm, 10.40 mm²

RISC-V Roadmap



Digital Autonomy with RISC-V in Europe



dare Roadmap for EuroHPC RISC-V SC

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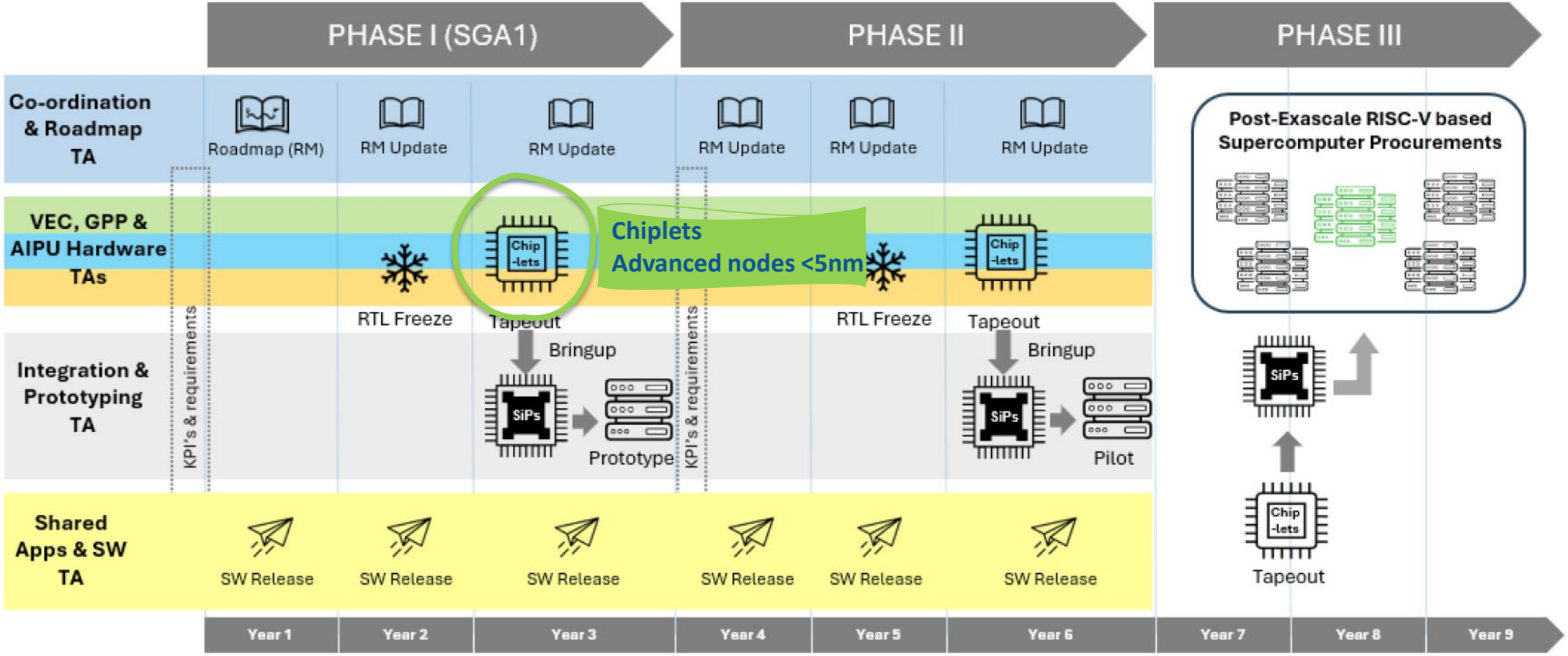


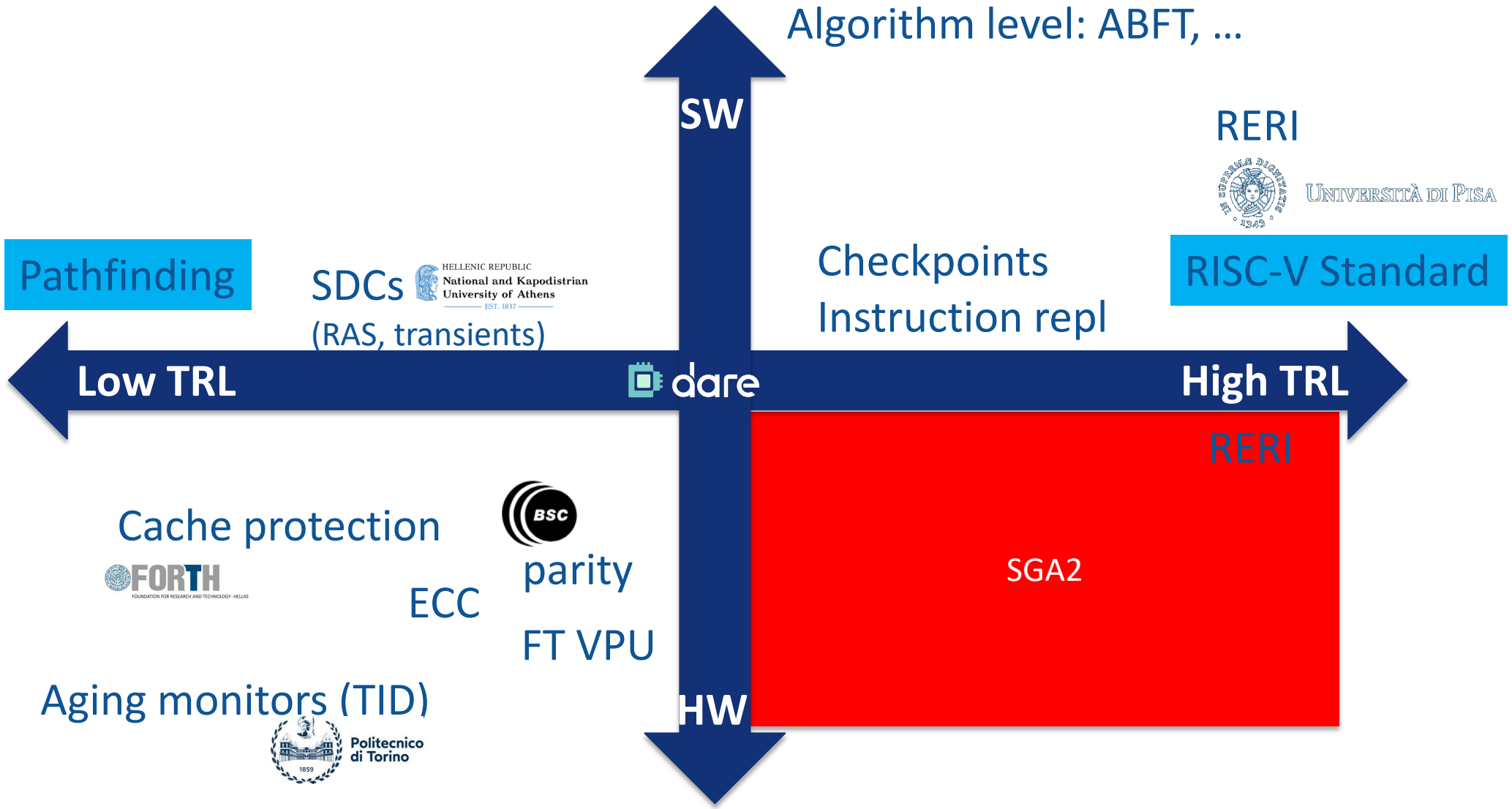
Fault tolerance at HPC

- Some similarities with (aero)space electronics
  - DRAM faults, aging errors, permanent faults, transients, SDFs …
  - Silent Data Corruptions (SDCs)
    - Radiation, electrical marginalities, silicon defects
    - Propagate to higher layers
- Different mitigation techniques
  - Mitigation / FT at HW level (expensive)
    - HPC standard: Mitigation at SW level: e.g. ABFT, ECC

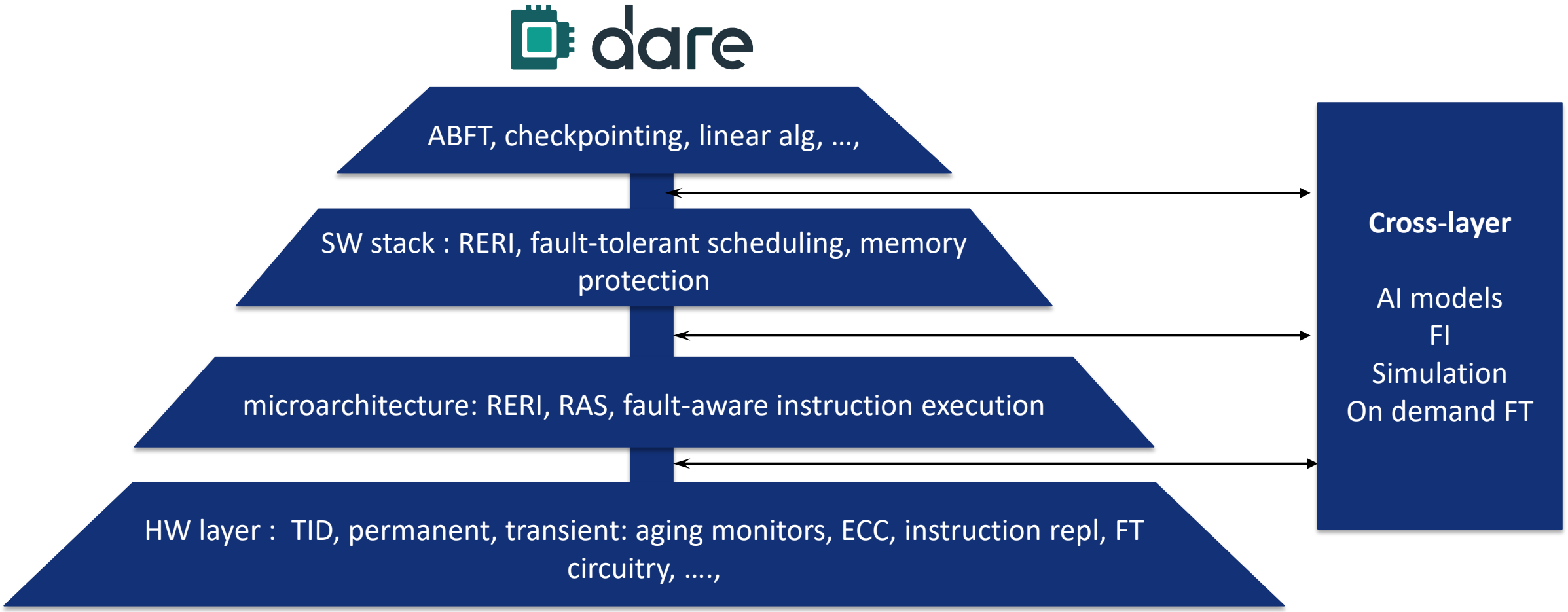
Fault tolerance at HPC

- Fault tolerance: not a standard in HPC so far
  - MTBF / core : 100 years -> JUPITER Supercomputer (1,7M cores)
    - **1 failure / 47 minutes**
- Proposed target approaches
  - HW-SW co-design approaches
  - Cross-layer reliability
  - AI-enhanced, simulation-based models for test
  - **Pathfinding track**

Fault tolerance pathfinding



Fault tolerance pathfinding



DARE SGA1 Technical Areas

BSC Coordination
(Roadmap, Technical Coordination, PMO, Diss & Inn)

JSC & BSC Shared Software

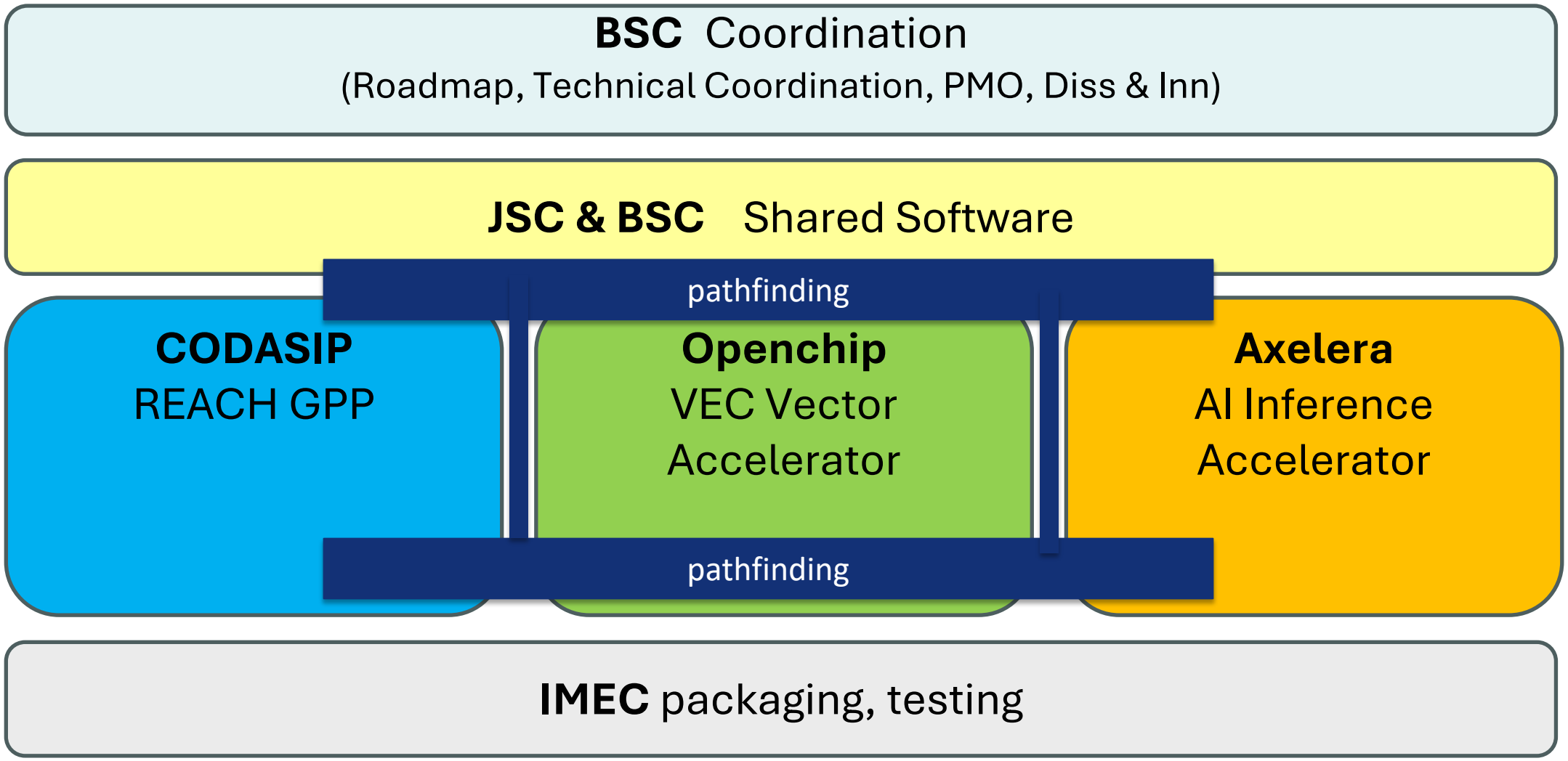
CODASIP
REACH GPP

Openchip
VEC Vector
Accelerator

Axelera
AI Inference
Accelerator

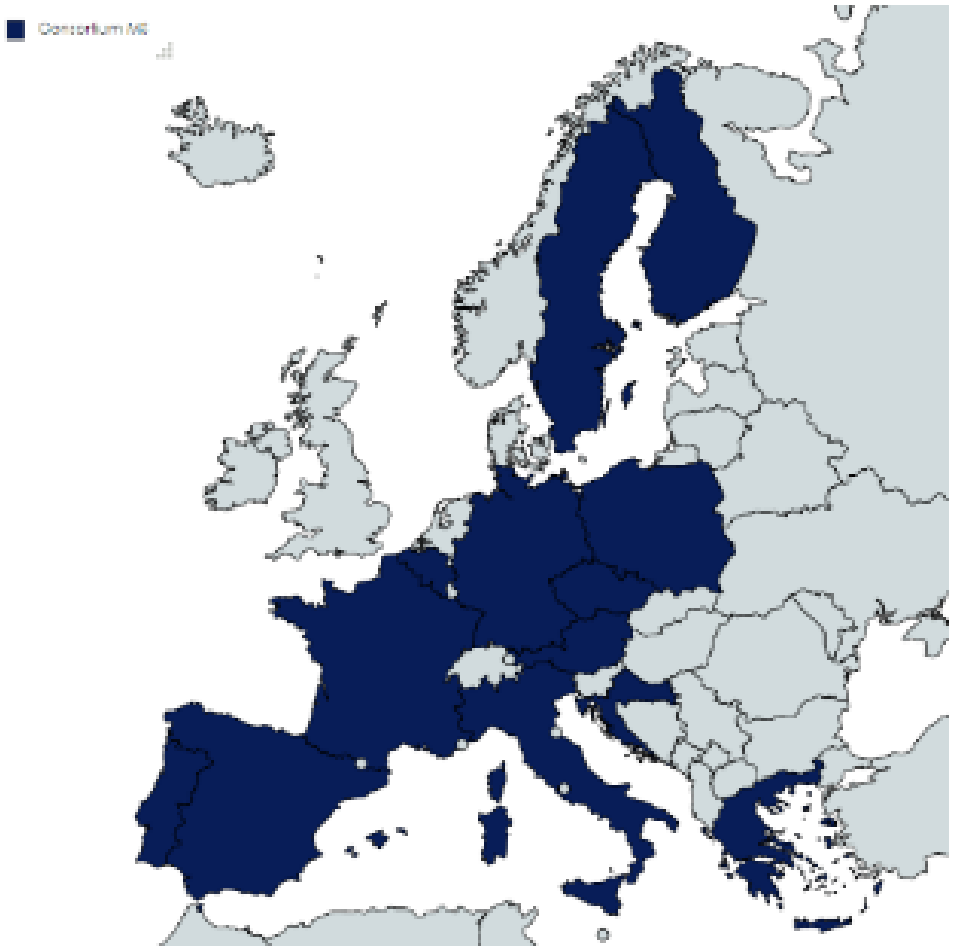
IMEC packaging, testing

DARE SGA1 Technical Areas



DARE FPA Partners

1. BSC, ES
2. AXELERA AI, IT
3. BULL, FR
4. CEA, FR
5. Chalmers, SE
6. CINECA, IT
7. CODASIP, DE
8. Cortus, FR
9. CSC, FI
10. CYFRONET, PO
11. E4, IT
12. ECMWF, Int
13. EXAPSYS, HE
14. Extoll, DE
15. FORTH, HE
16. FRAUNHOFER, DE
17. NKUA, HE
18. ICSC, IT
19. IMEC, BE
20. INESC-ID/IST, PT
21. INRIA, FR
22. IT4I (VSB), CZ
23. JSC, DE
24. KTH, SE
25. Leonardo, IT
26. Megware, DE
27. (NTUA) Athens, HE
28. Openchip, ES
29. ParTec, DE
30. RISE, SE
31. Silicon Austria Labs, AT
32. Sipearl, FR
33. TAU, FI
34. Thales (France), FR
35. Thales Alenia Space Italia, IT
36. TUM, DE
37. UNIBO, IT
38. Uni Complutense Madrid, ES
39. Uni Politècnica València, ES
40. University of Munchen, DE
41. UNIZG-FER, CR



Conclusions

- RISC-V is **inevitable**!
  - **Inclusiveness** in participating in actions from academia and industry
  - **Cutting edge technology and nodes**
- Faults in HPC systems are **inevitable!**
  - **Knowledge transfer** from space community to increase FT in HPC
- Consolidated effort of projects
  - develop tech diversity
- Clear, ambitious **vision** & roadmap

The European High Performance Computing Joint Undertaking

LEADING THE WAY IN EUROPEAN SUPERCOMPUTING

April 2025 | **Alexandra Kourfali**

THANK YOU

EuroHPC
Joint Undertaking

For more information, feel free to visit our website and social media:

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