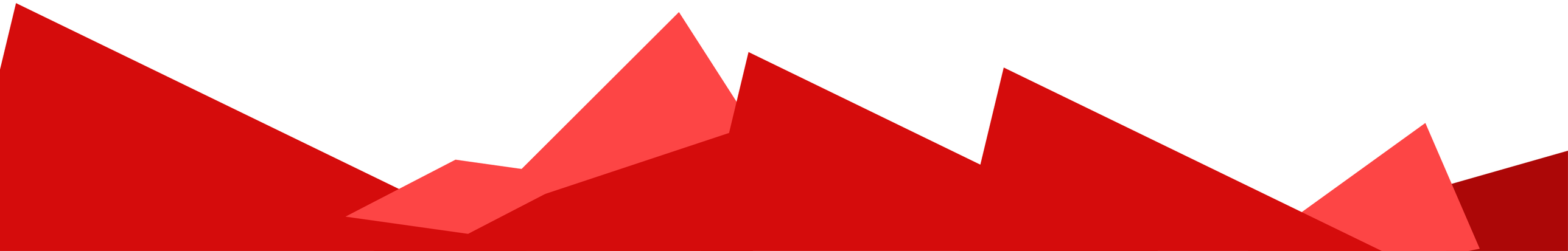
Full System Modeling and Simulation for RISC-V Platform Co-Design

John Leidel
Chief Scientist

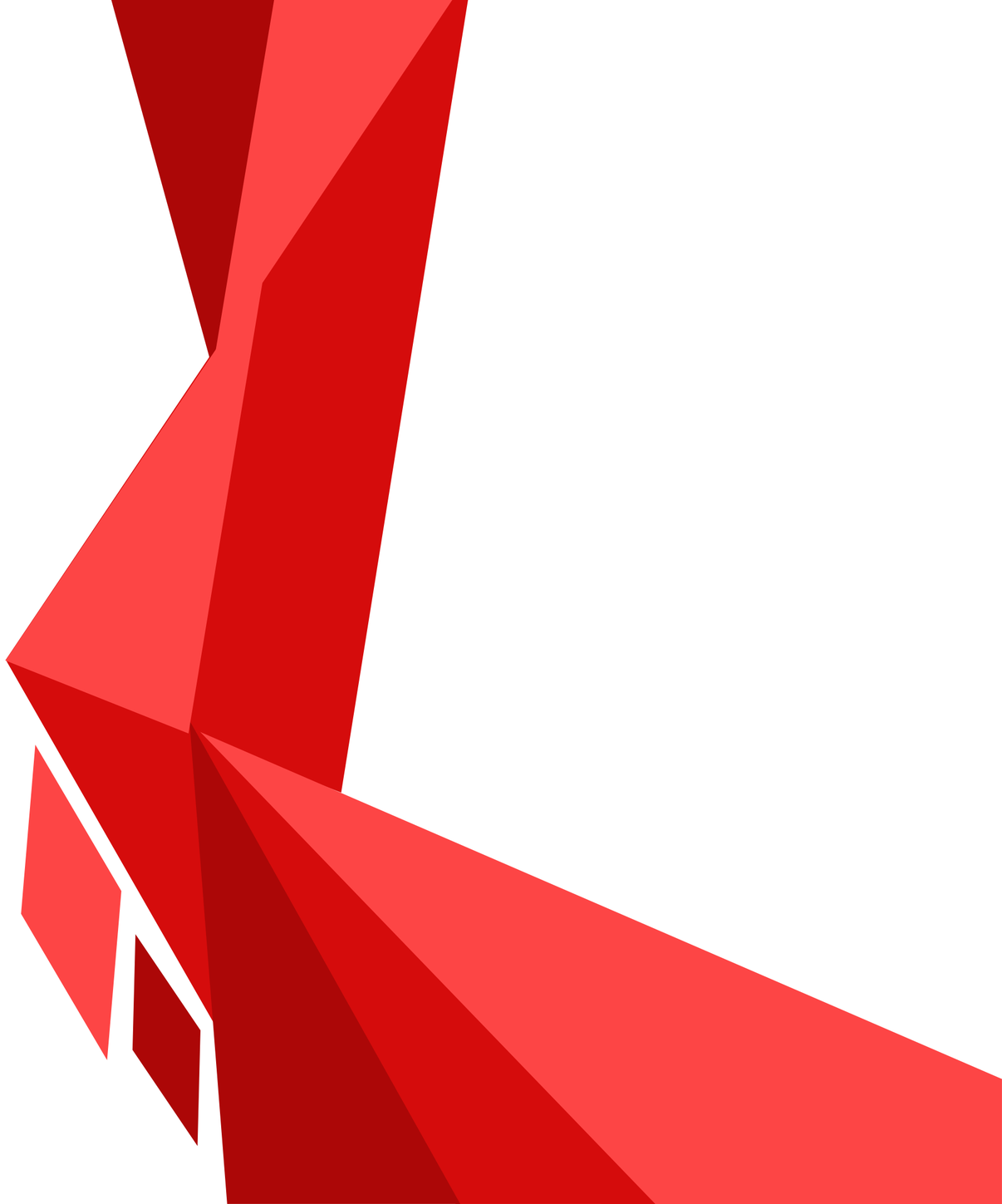
tactcomplabs.com

Outline

- *Who is TCL?*
- *Full System Modeling & Simulation for Co-Design*



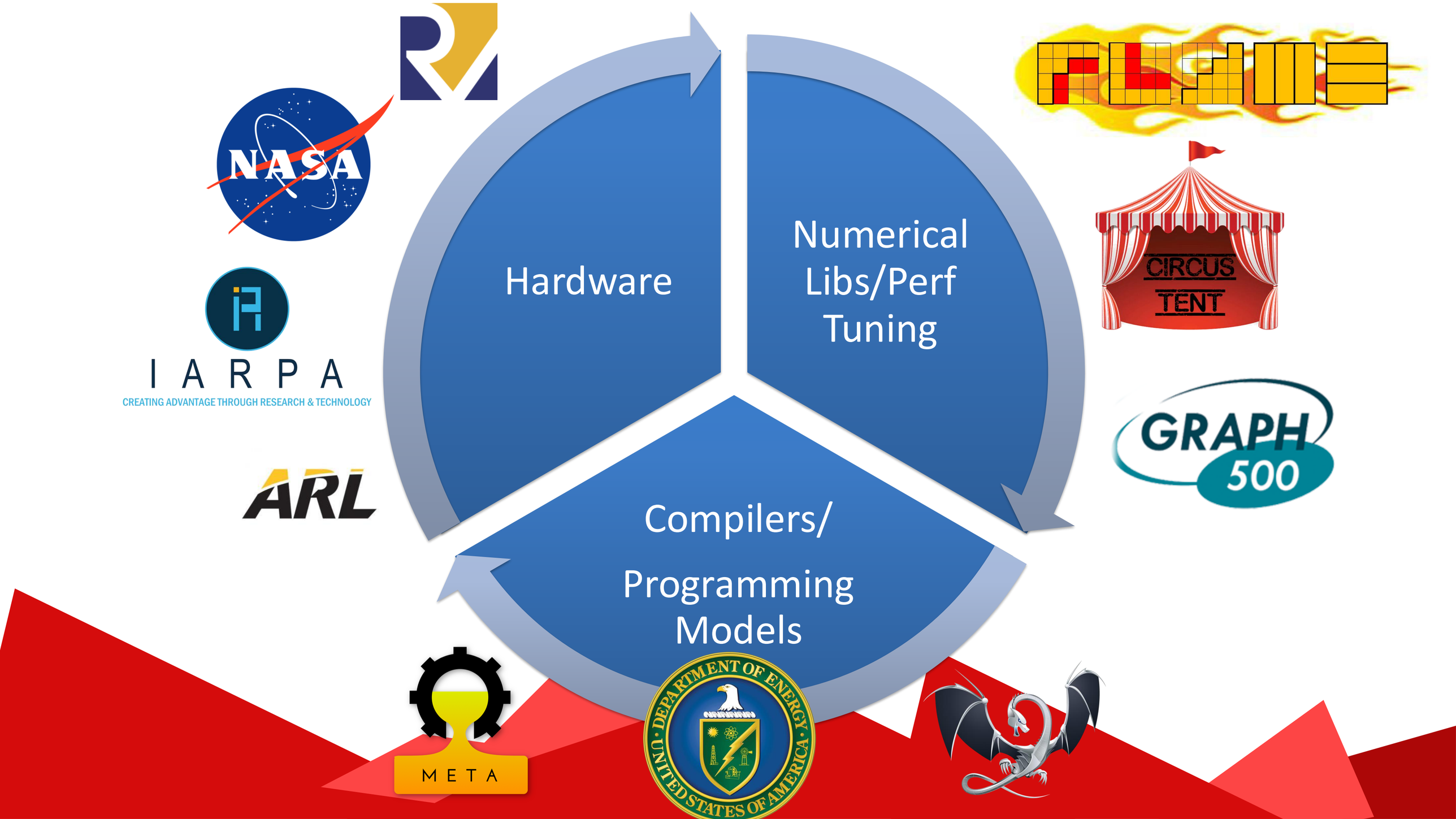
Who is TactCompLabs



History of TactCompLabs

- Founded in 2016 as a private research and development firm
- Private “think-tank” for advanced computing projects
- Clients in HPC, AI/ML, US Govt and space industry
- Dr. John Leidel
  - Found & & Chief Scientist
  - ~25 years of experience in HPC
  - Leads compiler development, system software, performance analysis and application development
- David Donofrio
  - Chief Hardware Architect
  - ~25 years of experience in FPGA + ASIC design
  - Former architecture lead at Lawrence Berkeley National Lab
  - Leads hardware, design tool and micro architecture development

Goal: ***Change the face of high performance computing by merging traditional software and hardware design and development***


Hardware
Numerical Libs/Perf Tuning
Compilers/ Programming Models
NASA
IARPA
CREATING ADVANTAGE THROUGH RESEARCH & TECHNOLOGY
ARL
CIRCUS TENT
GRAPH 500
META
DEPARTMENT OF ENERGY
UNITED STATES OF AMERICA

Full System Modeling & Simulation for Co-Design

Stages of ISA Modification (The Kathy Yelick paradigm)

Traditional Co-Design

xBGAS

Specification

RISC-V Extended Addressing
Architecture Extension Specification
Codenamed: xBGAS

Implementation

```
// Write handling
always @(posedge clk or negedge resetn) begin
    if (!resetn) begin
        memory.delete();  // Clear memory on reset
    end else if (i_mem_req_valid && o_mem_req_ready && i
        // if memory isn't initialized, initialize it
        if (!memory.exists(i_mem_req_data.addr)) begin
          memory[i_mem_req_data.addr] = {8{uninit_mem}};
        end
        // Process write request
        for (int i = 0; i < 8; i++) begin  // Handle all
          for (int j = 0; j < 8; j++) begin  // Handle a
            if (i_mem_req_data.be[i*8 + j] != 0) begin
                memory[i_mem_req_data.addr][((i*8+j)*8)
                //$display("HBM Write: Addr=%h, Data=%h"
            end
          end
        end
    end
end
```

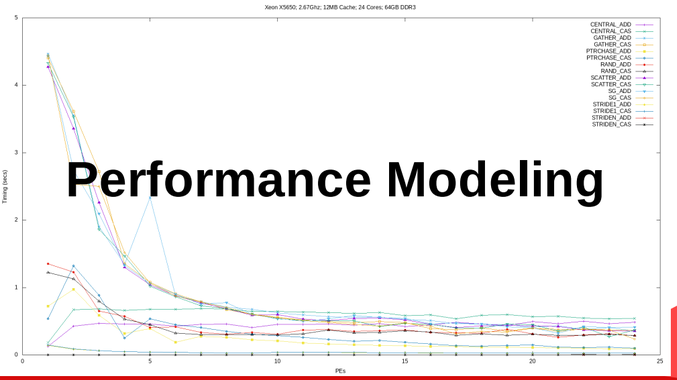
Performance Tuning

Algorithm 8: Scatter/Gather Kernel

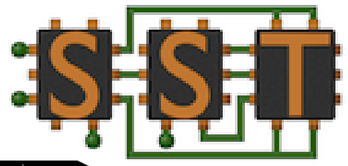
for $i \leftarrow 0$ **to** *iters* **by** 1 **do**
    src = AMO(IDX[i])
    dest = AMO(IDX[i+1])
    val = AMO(VAL[src])
    AMO(VAL[dest], val) // VAL[dest] = val
end

Modeling & Simulation

Performance Modeling



Full System Co-Design



Modeling & Simulation

RTL Implementation

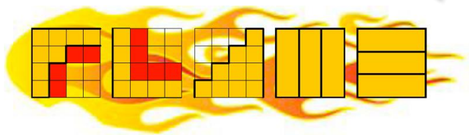
VERILATOR

Specification

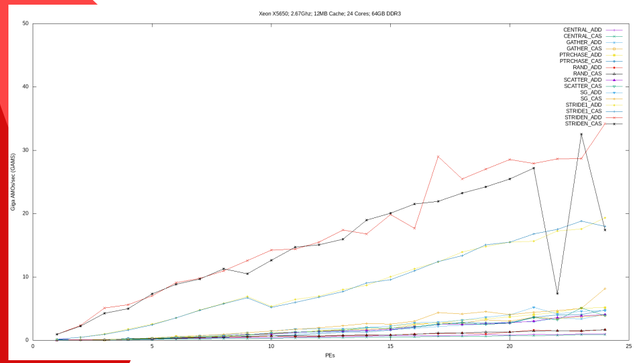
Compiler/Programming Model Implementation

kokkos

Performance Tuning

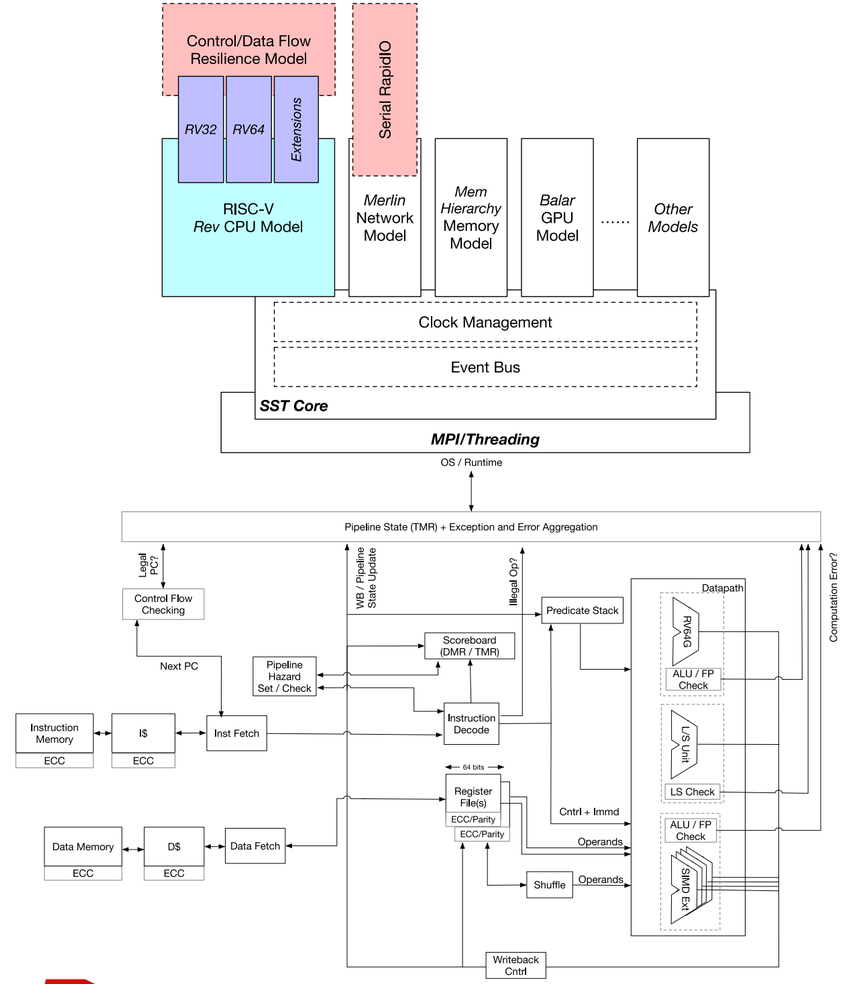


Performance Modeling



Co-Design for Space: RADRISC

- NASA SBIR project to investigate deploying RISC-V for mixed space flight operations
  - In-flight telemetry/navigation
  - Onboard scientific experiments
  - Autonomous vehicles/satellites
- Full system simulation infrastructure using SST parallel simulator
  - RISC-V, network models, memory models
  - Tunable radiation attack modeling
- Fully integrated RTL models
- Sim/RTL Software infrastructure with cross compatibility




TCL