Ultra-Deep Submicron Technologies for European Space Sovereignty

Advancing Next-Generation Processors and System Integration

Boris Glass
03 April 2025

Outline

- European Space Agency
- European Sovereignty and Supply Chain
- UDSM Activities
- IP Building Blocks
- Development Plan

23 Member States

1 Long-standing Cooperating State

4 Associate Members

INSIDE ESA

Four pillars. One ESA.

SCIENCE

SPACE TRANSPORTATION

EARTH OBSERVATION

NAVIGATION

COMMERCIALISATION, INDUSTRY & COMPETITIVENESS

HUMAN & ROBOTIC EXPLORATION

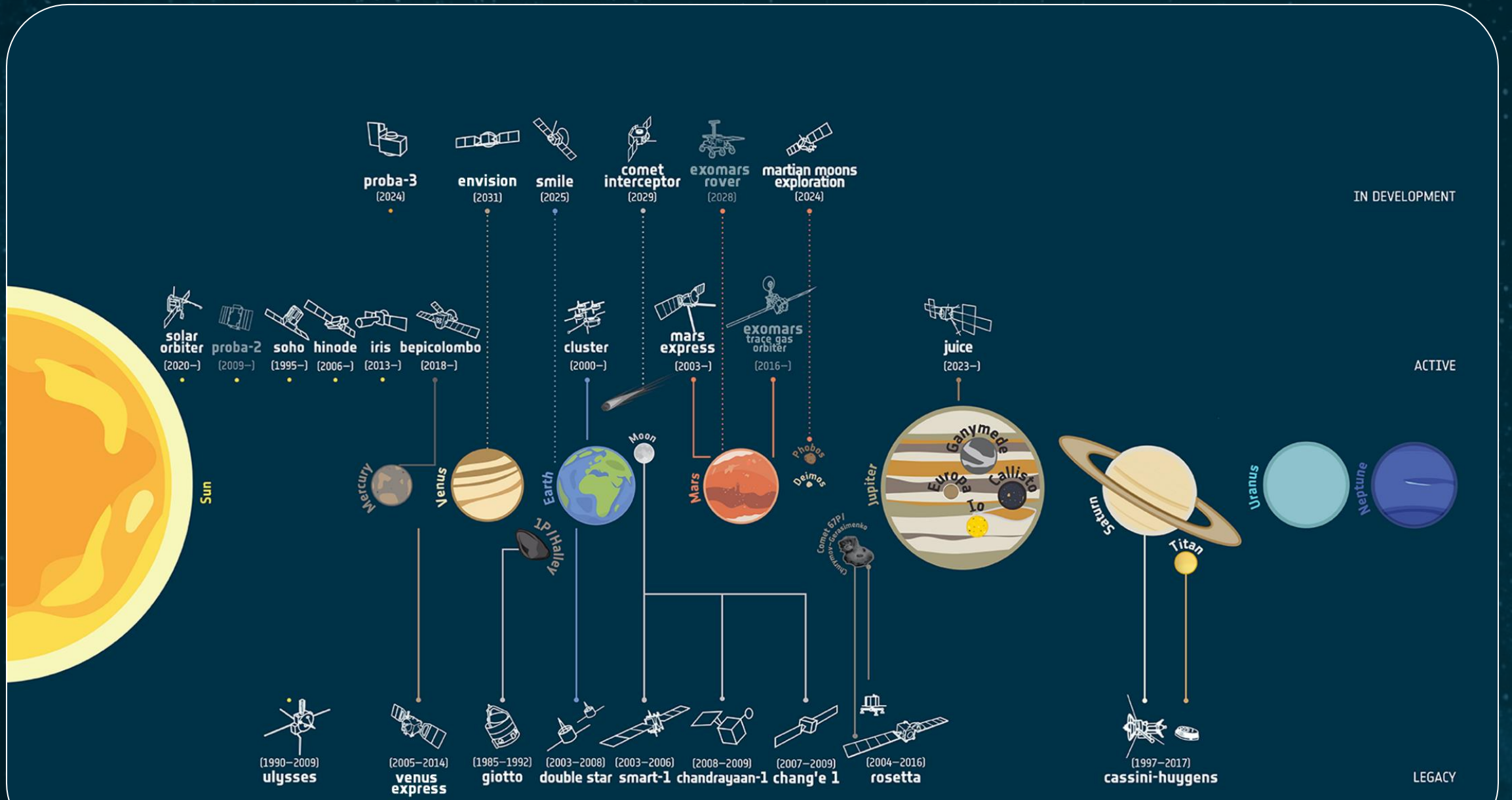
OPERATIONS

TECHNOLOGY

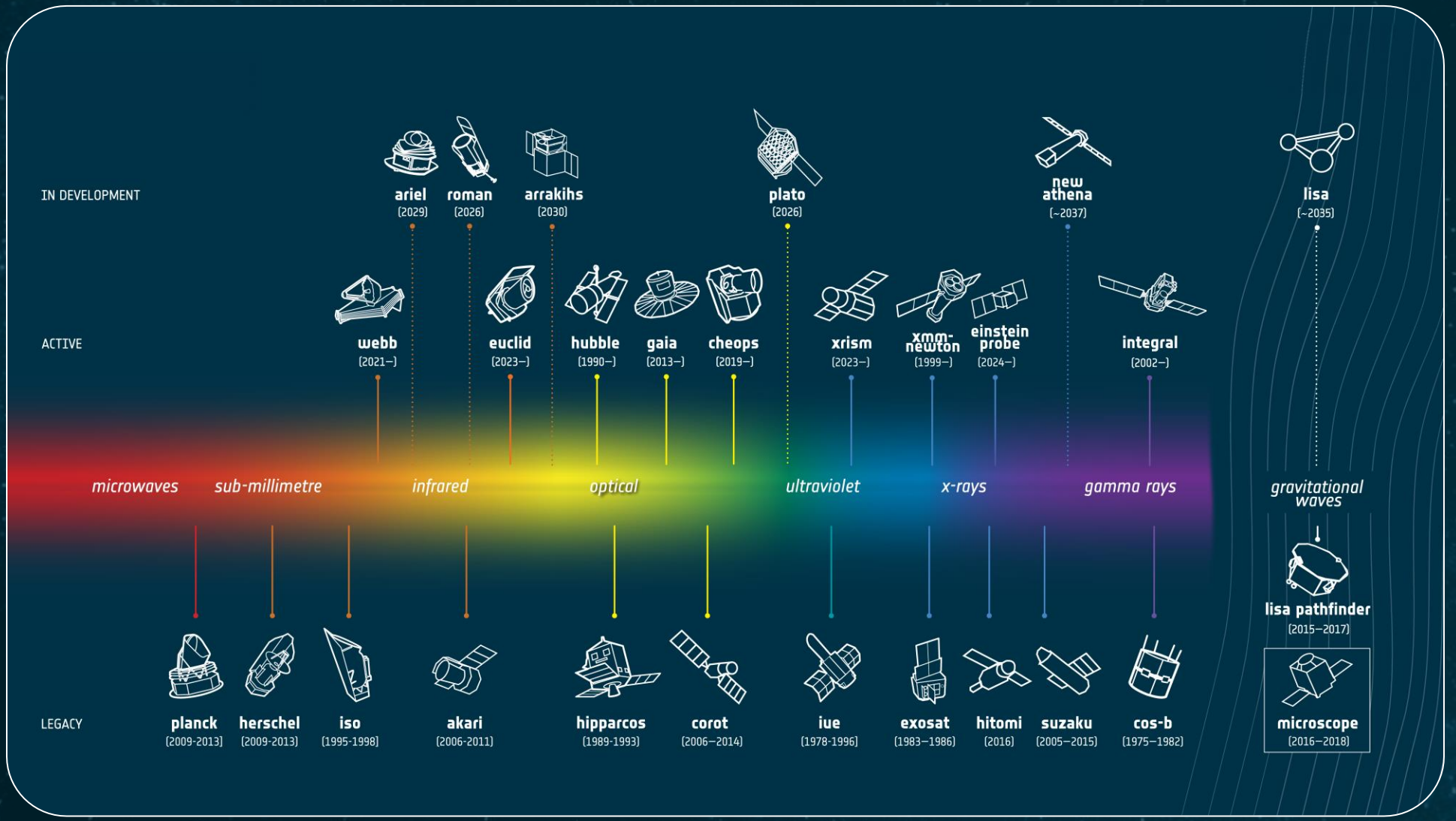
CONNECTIVITY & SECURE COMMUNICATIONS

SPACE SAFETY

Solar System Explorers

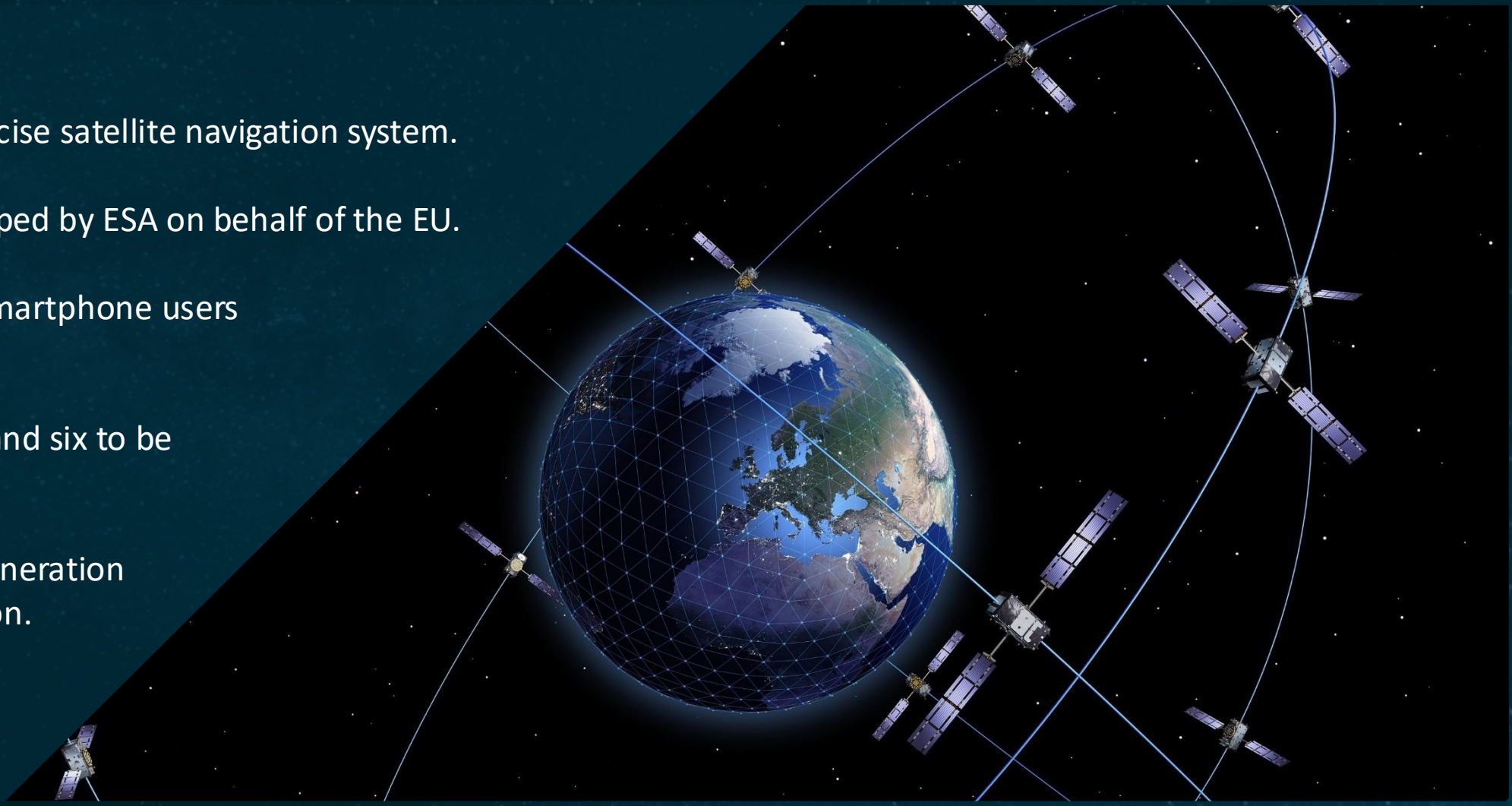


Cosmic Observers



Galileo

- The world’s most precise satellite navigation system.
- Designed and developed by ESA on behalf of the EU.
- Serving four billion smartphone users around the globe.
- 32 satellites in orbit and six to be launched
- 12 Galileo Second Generation satellites in production.



FutureNAV

Designing new missions and responding to new satnav trends and concepts for improved positioning, navigation and timing (PNT) services.

Two initial missions:

- LEO-PNT: In-Orbit-Demonstration mission of low Earth orbit PNT services
- GENESIS: A single satellite flying four key Earth-measuring technologies

ARTES: fostering innovation and competitiveness

ESA's programme of Advanced Research in Telecommunications Systems (ARTES) fosters innovation to enable the European and Canadian space industry to succeed in highly competitive global markets.

Strategic programme lines:

- Space for 5G/6G
- Optical and Quantum Communications (ScyLight)
- Space systems for safety and security

Infrastructure for Resilience, Interconnectivity and Security by Satellite (IRIS²)

ESA is working with the EU to deliver a highly secure, satellite-enabled connectivity system called IRIS².

ESA, the EU and European industry are partnering to deploy IRIS², Europe's flagship space programme for sovereign, resilient and secure satellite communications.

IRIS² involves an advanced multi-orbit constellation, featuring software-defined payloads that enable efficient and advanced broadband communications worldwide.

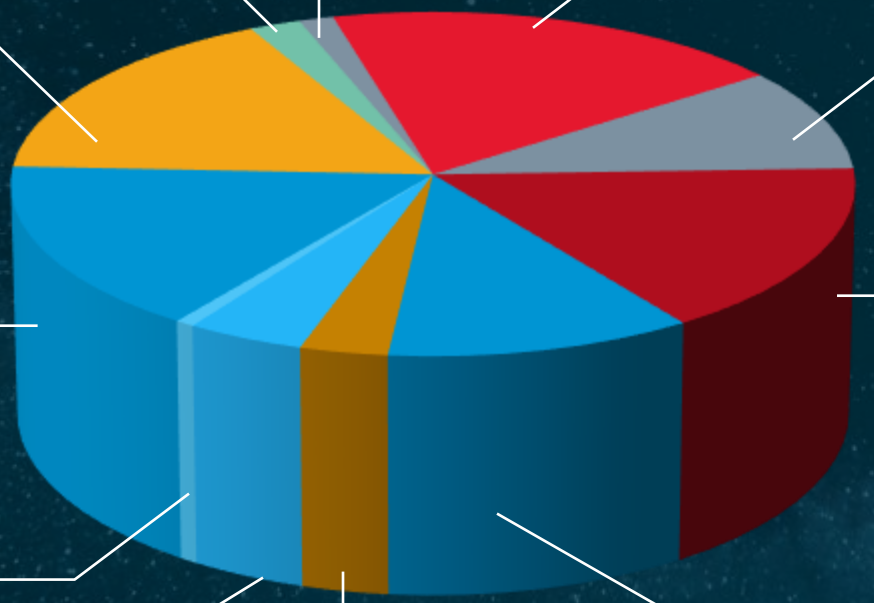
Moonlight

- Over the next two decades, space agencies, companies and research institutions plan to launch hundreds of missions to the Moon. Working with industrial and institutional partners, ESA is developing Moonlight, a constellation of satellites offering navigation and telecommunications services to support these missions and
allow them to focus on their core objectives.

- Moonlight will establish reliable, autonomous communication and navigation infrastructure, supporting a sustainable return to and long-term presence on the Moon. As such, Moonlight will make previously unfeasible missions possible, paving the way for the future internet of the Universe.

Total subscriptions €16.9 billion, agreed at CM22, **(+17%)**

Mandatory activities and CSG for five years



NAVIGATION
€351 million, 2%

PRODEX
€237 million, 1%

SCIENTIFIC PROGRAMME
€3186 million, 19%

SPACE TRANSPORTATION
€2835 million, 17%

BASIC ACTIVITIES
€1629 million, 10%

EARTH OBSERVATION
€2693 million, 16%

HUMAN & ROBOTIC EXPLORATION
€2707 million, 16%

COMMERCIALISATION, INDUSTRY & COMPETITIVENESS
€118 million, 1%

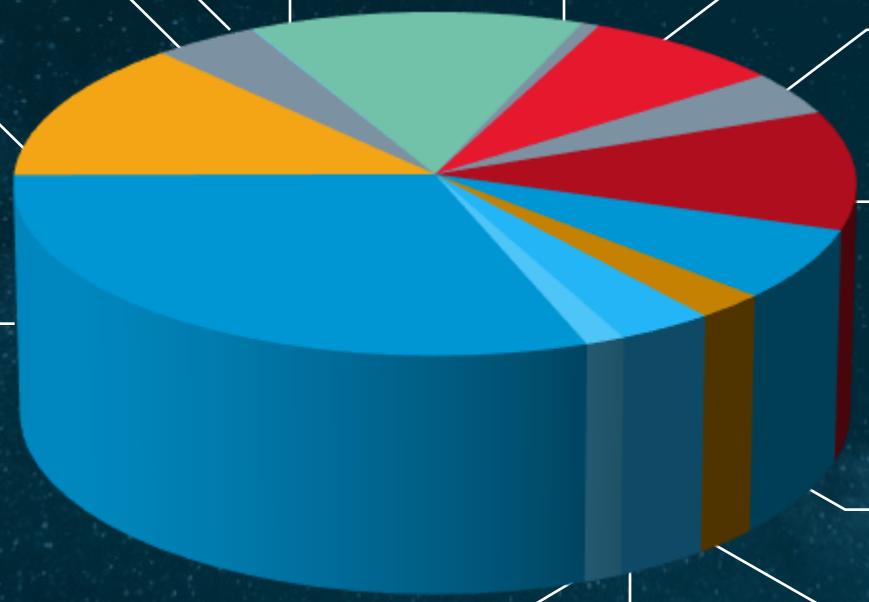
SPACE SAFETY
€731 million, 4%

TECHNOLOGY
€542 million, 3%

CONNECTIVITY & SECURE COMMUNICATIONS
€1894 million, 11%

Annual budget* 2024 (by domain)

TOTAL: €7.79 B** (+10% vs. 2023)



NAVIGATION
€1051.1 million, 13.5%

EUROPEAN COOPERATING STATES AGREEMENT
€5.9 million, 0.1%

PRODEX
€56.6 million, 0.7%

SCIENTIFIC PROGRAMME
€632 million, 8.1%

ASSOCIATED WITH GENERAL BUDGET
€330.1 million, 4.2%

BASIC ACTIVITIES
€322.9 million, 4.1%

SPACE TRANSPORTATION
€1032.7 million, 13.3%

HUMAN & ROBOTIC EXPLORATION
€873.8 million, 11.2%

EARTH OBSERVATION
€2372.4 million, 30.5%

CONNECTIVITY & SECURE COMMUNICATIONS
€525.7 million, 6.8%

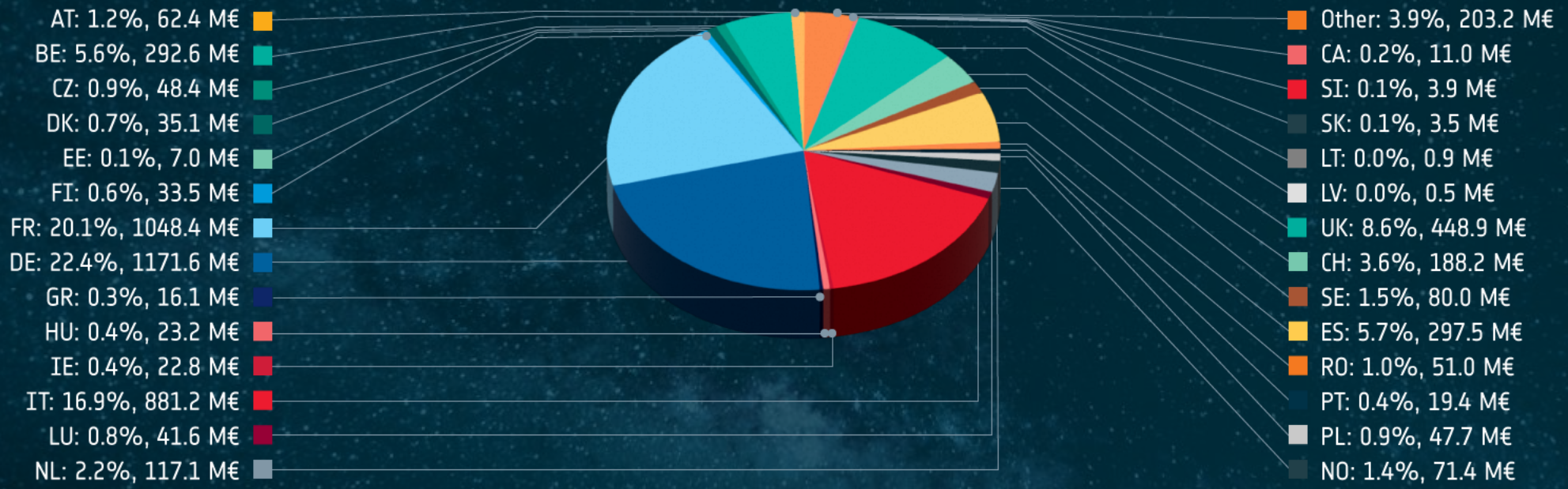
COMMERCIALISATION, INDUSTRY & COMPETITIVENESS
€111.8 million, 1.4%

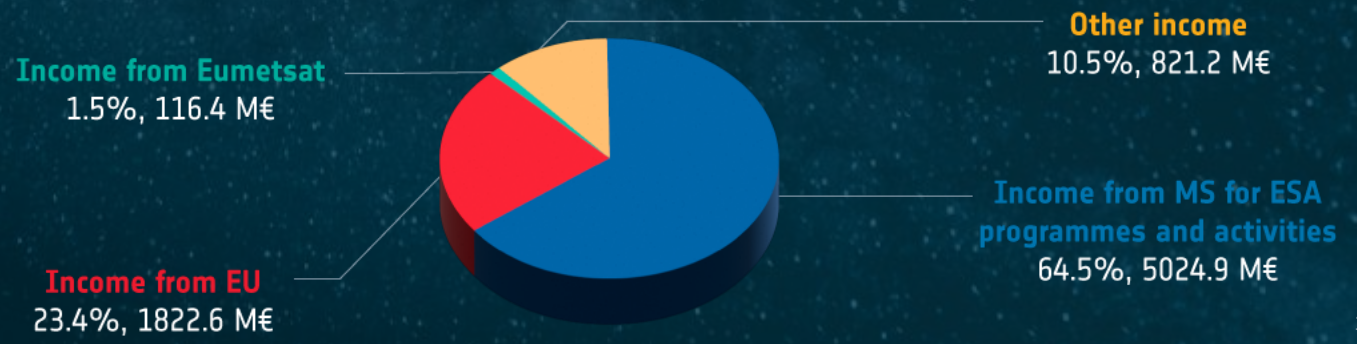
TECHNOLOGY
€196.7 million, 2.5%

SPACE SAFETY
€273.4 million, 3.5%

*Adopted budget, not final budget **Includes activities implemented for other institutional partners

Annual budget, 2024 (by funding source)



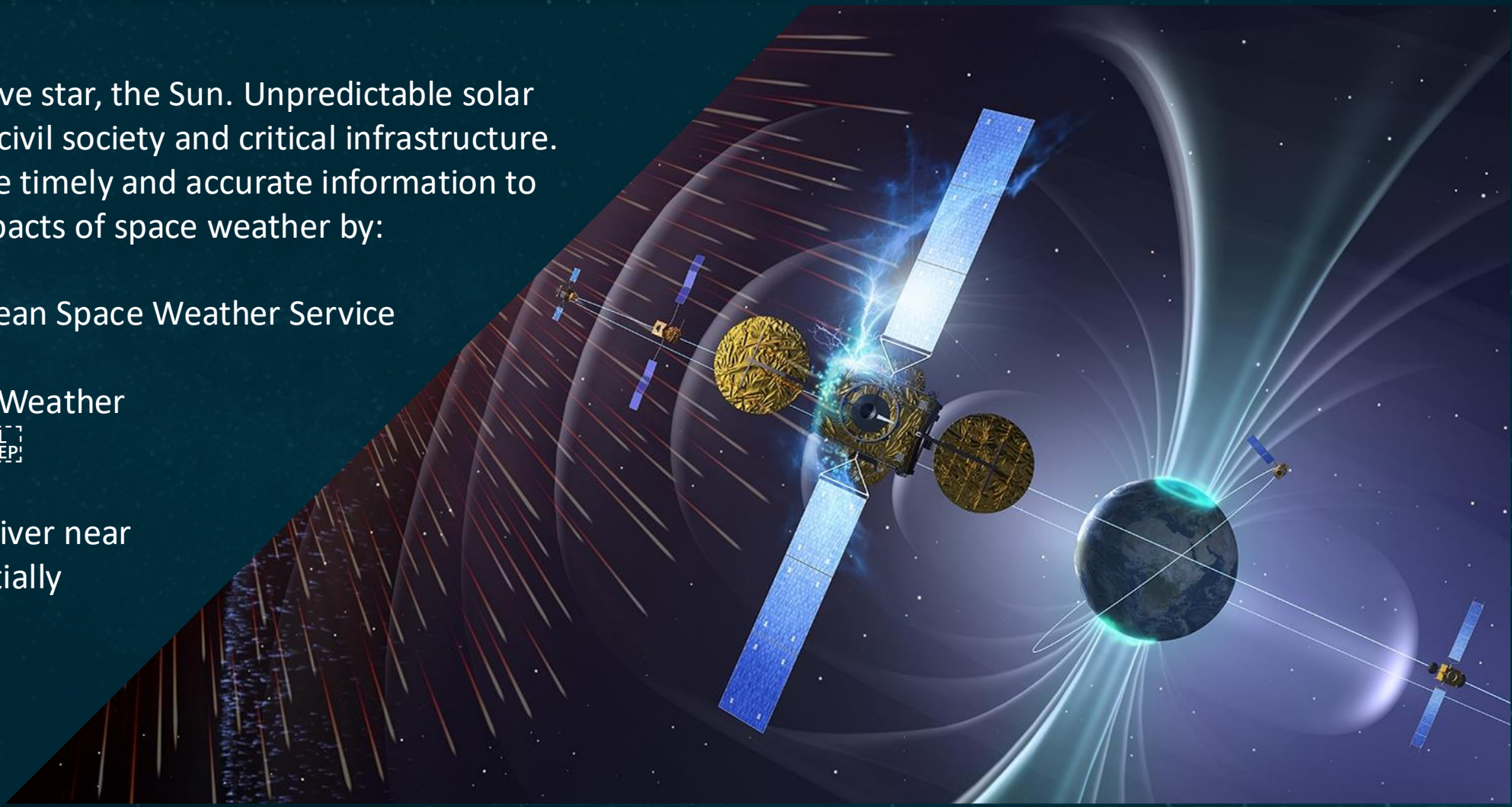


Space weather

Our planet orbits an active star, the Sun. Unpredictable solar emissions pose a risk to civil society and critical infrastructure. ESA is working to provide timely and accurate information to mitigate the adverse impacts of space weather by:

- enhancing our European Space Weather Service Network, and
- upgrading our Space Weather Coordination Centre (SEP)

The Vigil mission will deliver near real-time data on potentially hazardous solar activity before it is detectable from Earth.



1: Vision – European Sovereignty

Sustainable products, no access restrictions

Increase European competitive-ness

Strong European Supply Chain

Strategic partnerships

Time-to-market of qualified products

Introduction

Background

The EEE Space Component Sovereignty for Europe was approved at CMIN22 as a GSTP Component

Objective

The main goal of the EEE Initiative is to facilitate the provision of European Components, through strong supply-chains, to ESA and European Space Industry in time, to cost, at the right maturity level and with no restrictions

Achievements

Several high-value activities to develop state-of-the-art European technologies have been initiated as presented at the CMIN22 and subsequent IPCs

Expectations

Availability of competitive European EEE products in time, at the right maturity level and ESCC qualified.

Through PPP, industry driven sustainable European supply chains.

Capture European and international multi-use markets “not because the products are European but because they are competitive”

Collaboration

With National Agencies

Under the umbrella of the GSTP Component, EEE Initiative activities are closely discussed with Member State delegations, and through strong networks coordination with national programmes are oursued.

With EC

Collaboration and coordinate with EC through JTF, and dedicated technology coordination Tiger Team (i.e. for FPGAs, potentially expandable to other EEE Technologies)

With Industry

Great efforts are excreted to align technology needs and product strategies (e.g. related to volume, performance and multi-usability)

Proposal

Ensure **time-to-market** of products initiated after **CMIN22**, replace **non-European integrated Circuits** in ESA missions and introduce the **Passive component family**

Collaborative approach

- Strong synergy with European Space Component Coordination (**ESCC**) /Component Technology Board (**CTB**)
- ESCC CTB roadmaps and Harmonisation roadmaps fully considered as a basis, but with additional supporting information (business case, quantified space system performance benefits, etc.)
- Coordination with National Agencies, **EC**, **EDA** using existing channels (e.g. **JTF**)
- No direct link to European Chips Act however with expectations that there will be synergies
- Working Arrangement between ESA and EC on the Coordination of Security Critical Electrical, Electronic and Electro-mechanical Components (**SecEEE**)

National and European Collaboration

- **In cooperation with National Space Agencies**
  - Supporting company UDSM N7 product development
    - Increase competitiveness of final product
    - Reduce development and manufacturing costs with co-operation
    - Reduce development risk for UDSM prototypes with co-operation
    - Establishing sustainable supply chain
  - Support to National UDSM Technology Teams
  - Preparing companies for European UDSM ITTs as part of the supply chain

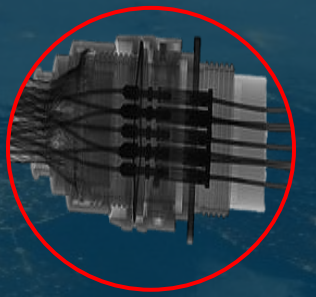
- **Cooperation with EC**
  - Joint Task Force
    - Identification of product and technology development priorities, budgets
  - Tiger Team
    - Alignment of development schedule for FPGA
    - Discussion on sharing of development funding for FPGA
  - Coordination Mechanism for Security Critical EEE Components technologies

Technology Lines for European Leadership

Test facilities

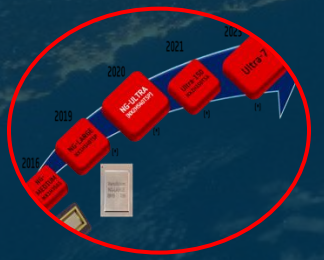
Packaging, PCB and EA

Passive

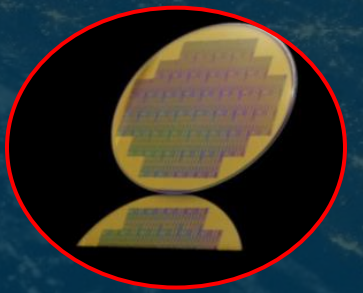


Technology Lines

UDSM



Wide Band-Gap (GaN/SiC)



Photonics

ESCC qualification

Status of EEE Initiative activities

EEE GSTP Component activities

- Ultra Deep Sub-Micron Foundation and Platform Technology
- Ultra Deep Sub-Micron Interface and System-in-Package Technology
- Development of Serializer and Deserializer IP Core for Ultra Deep Sub Micron Technologies

- Super Scaled Nitride Technology (S2CANT)
- Thermal Heat Reduction techniques for Semiconductor Technology (THRUST) – Phase 1

- European Power SiC supply chain (EPOSIC)
- GaN monolithic IC Pre-Industrialisation development – GaNICp

- Development of a High Energy Ions Beam Testing Capability (>22MeV/n)

51 MEuro supported. These activities are running, under negotiation or early phase of ITT process.

Achieving rapid time-to-market propels European industry into leading global positions

Cutting-edge European EEE component technologies support strategic European goals

Collaboration among European stakeholders is essential

EEE Initiative activities still to be started

EEE GSTP Component activities

- Packaging Solutions for UDSM and Photonics devices
- Packaging for Wide Band Gap RF devices

- Lead-free Electrical Assembly technology for high reliability electrical connections
- High speed Printed Circuit Board assemblies
- Thermal management for Printed Circuit Board assemblies

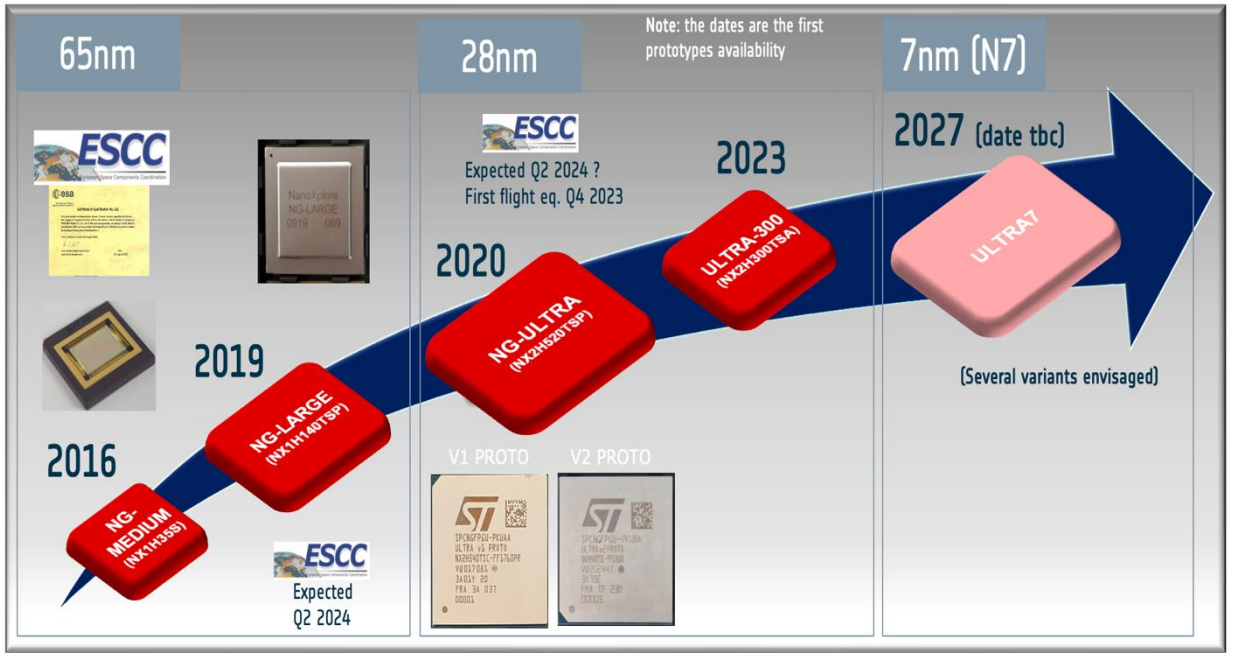
Some packaging activities are covered under other porgammes such as ARTES

Many Solar Cell related activities already running under other porgrammes , therefore not included here

A Laser Diode Module Wafer level Packaging is being prepared under the EEE initiative

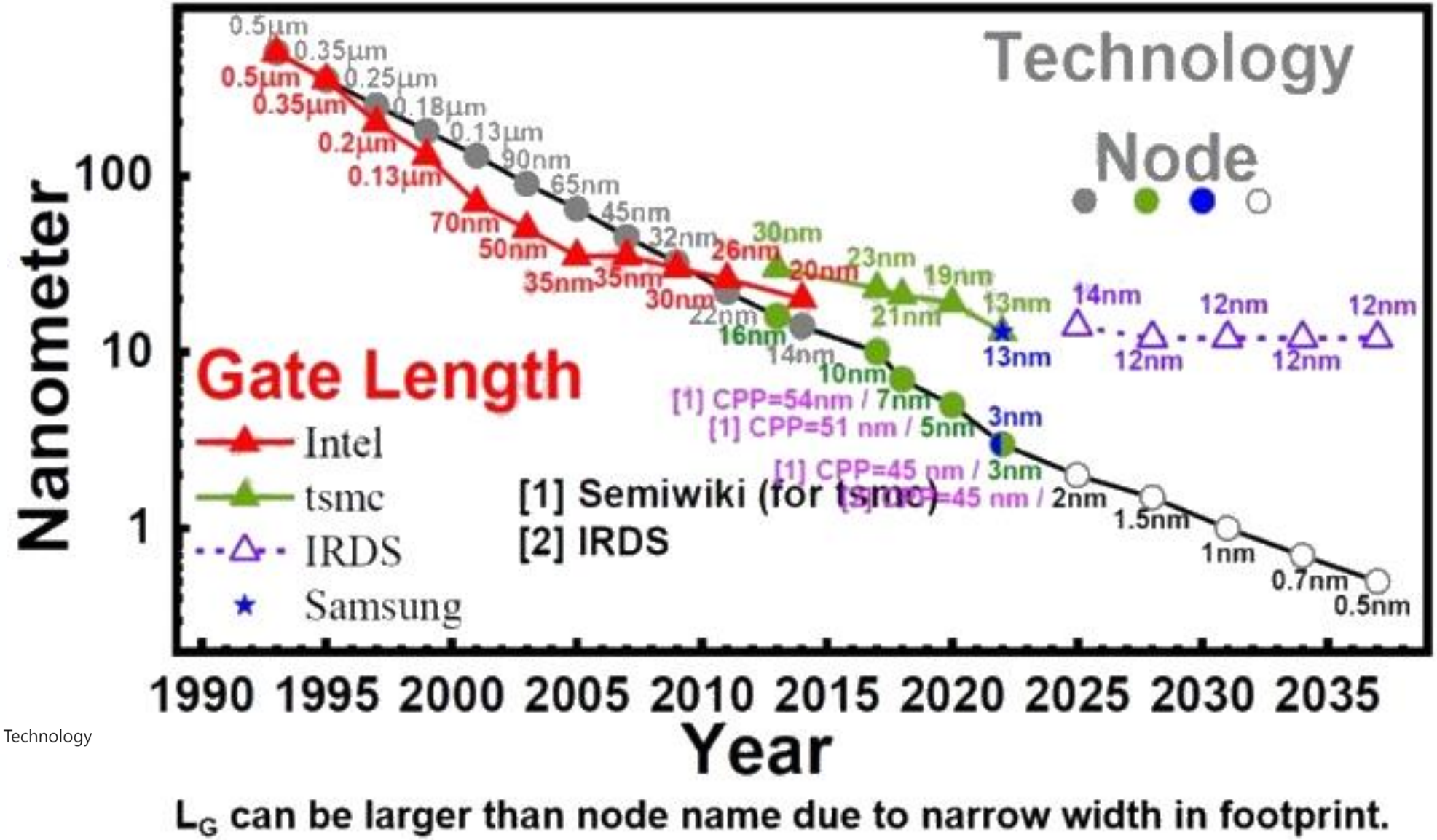
FPGA Development - Demonstrated Track Record

- 4 products in less than 10 years



In this context, there is a need to accelerate the development of European space FPGA based on 7nm (N7). The Commission and the European Space Agency should join forces and ensure complementarity and consistency between their respective activities. We should build upon the very good example of cooperation we put in place to support the development of FPGA based on 28nm, a few years ago.

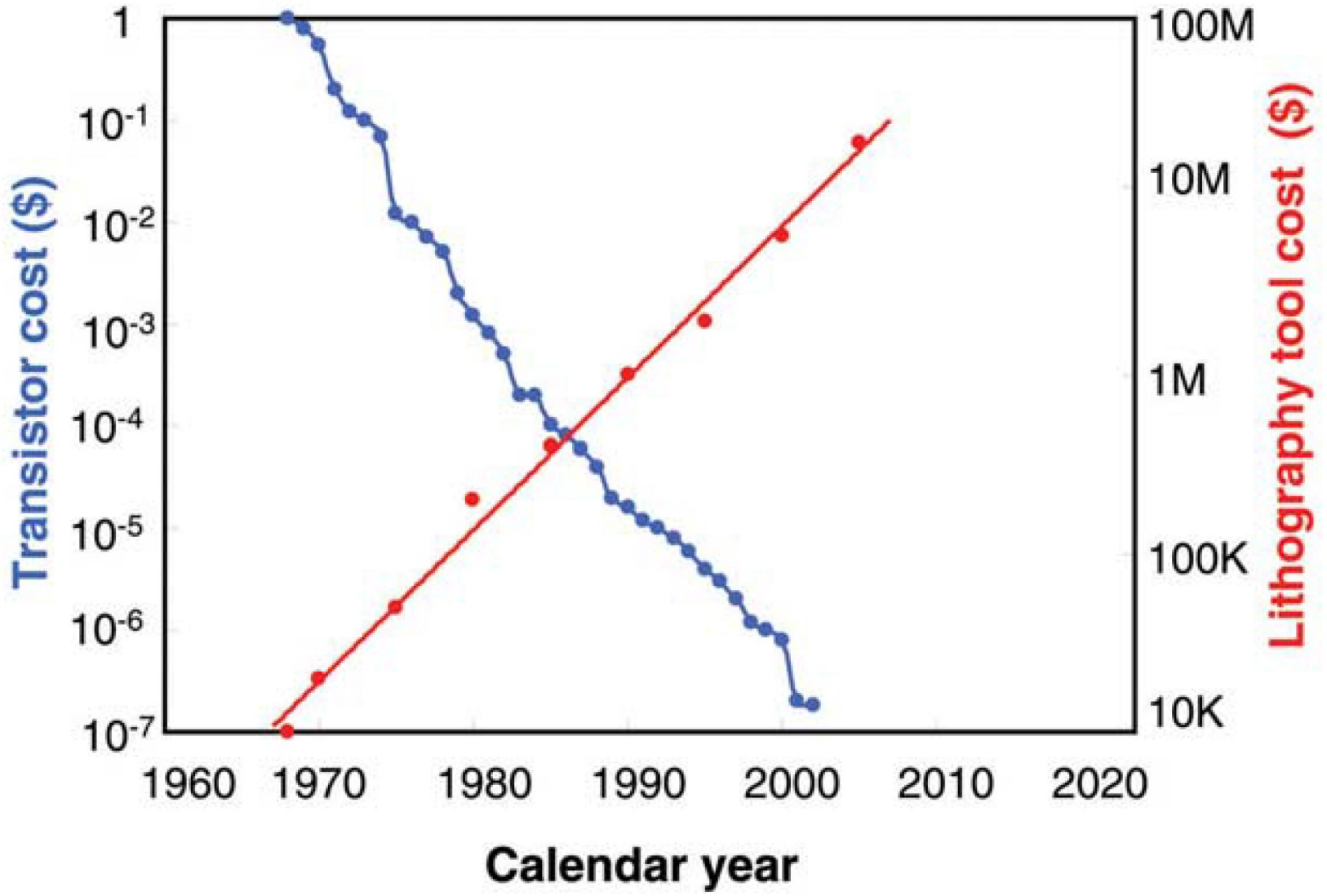
Technology Scaling – Gate Length Evolution



L_G can be larger than node name due to narrow width in footprint.

Sachidananda Dash
DRAM Product Engineer at Micron Technology
Sachidananda has verifications
Taichung City, Taichung City, Taiwan

Technology Scaling – Lithography Cost



Moore's law: the future of Si microelectronics

Scott E. Thompson ✉, Srivatsan Parthasarathy ✉

UDSM Technology Landscape

Foundries

Current in Europe

- ST – 28 nm FDSOI
- GF – 22 nm FDSOI
- Intel – Intel 7 FinFET (export restrictions)

Future in Europe

- ST – 18 nm FDSOI
- CEA-Leti – 7 nm FDSOI (under development)
- Intel – Intel 4 FinFET (export restrictions)
- ESMC – 12nm FinFET

Outside Europe

- TSMC – N7 FinFET (Taiwan)
- TSMC – N7 FinFET (Japan) (2nd Supply Option)
- TSMC – N4 FinFET (US)

Overview of the UDSM Foundries in Europe

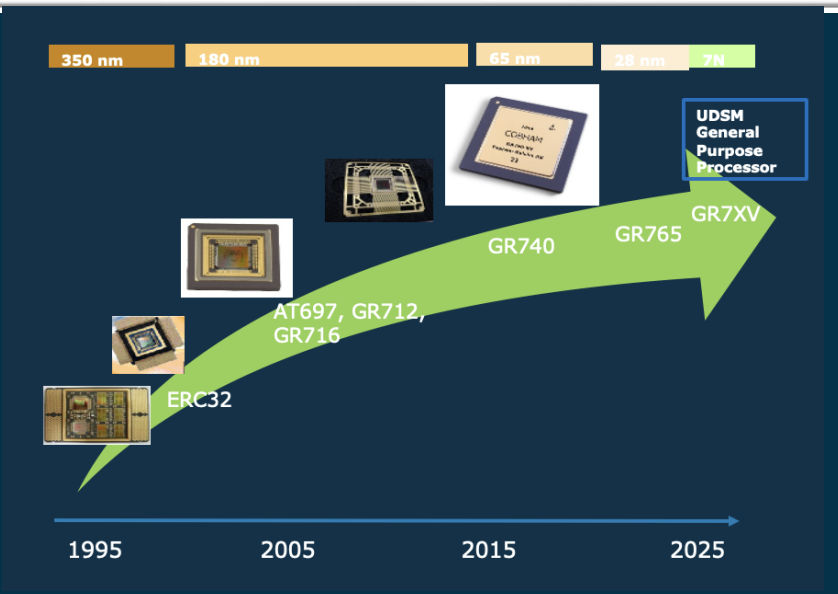
UDSM N7 Technology for Space Components/Applications

Space Components

- General Purpose Processor (GPP)
- Field Programmable Gate Arrays (FPGA)
- RF Direct Sampling Converters
- Digital Beamforming Front-ends
- Digital Signal Processors (DSP)
- Domain Specific Accelerators (DSA)

Space applications

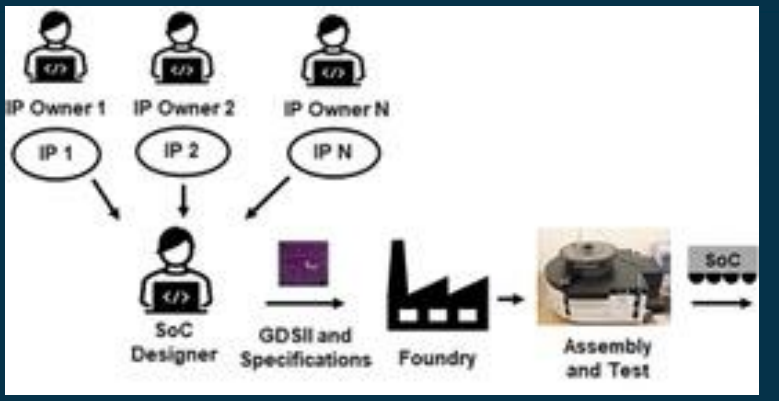
- Digital Beamforming Telecommunication
- Satellite Telecommunication
- Payload processors (SAR, Image Processing, …)
- Autonomous Systems
- Space AI Applications



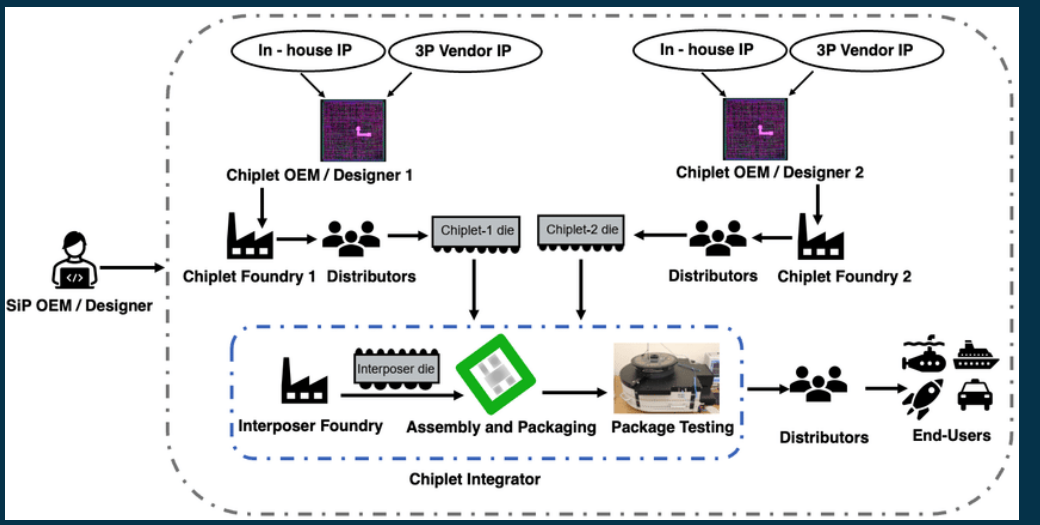
Field Programmable Gate Array Evolution

Supply Chain for the UDSM N7 Technology

- Supply Chain SoC Die/Chiplet
  - Foundry
  - Backend Service Provider
  - SoC Developer
  - IP Provider
  - CAD Tool Provider
- Supply Chain SoC Component
  - Component
  - Assembly, Packaging and Test
  - Package Provider
  - SoC Die/Chiplet Supply Chain
- Supply Chain SiP
  - SiP Component
  - Assembly, Packaging and Test
  - Interposer Provider
  - Supply Chain Chiplet



Overview of System on Chip (SoC) Supply Chain



Overview of System in Package (SiP) Supply Chain

Covered by EEE Component Sovereignty Initiative - UDSM Technology Line

Covered by EEE Component Sovereignty Initiative – Packaging Line

Support to UDSM N7 Product Developments

- **Support Development**
  - Strategic/Sustainable UDSM N7 Products
    - Generic and Application Specific
  - Supply Chain Actors (SoC Designer, IP Providers, Back-end Services, Packaging,)
- **Support National UDSM Technology Teams** (BE, DE, FR, IT, SE, UK, …)
  - Component Specification
  - IP Selection
  - Budgeting and Planning for Prototype
- **Derisk Application Specific UDSM N7 Product Development**
  - Telecom processors
  - Digital Beamforming Front-ends
  - Domain Specific Accelerators
  - …
- **Develop needed UDSM N7 IP and Backend services**
- **Ensure Access to IP for testchip/prototype validation**
- **Facilitate Manufacturing**
- **Support planning of UDSM N7 product development roadmap (prototype to flight parts)**
  - **funding (average 40Meuro per component)**
  - **schedule**
  - **collaboration**
- **Support complementary technology development**

Strategic/Sustainable UDSM N7 Products

- Support EEE component sovereignty
- Consolidate supply chain in ESA member states
- At least a two-fold return of investment of public funding

Ultra Deep Sub Micron – Activity Overview

UDSM 0 — Started

UDSM Assessment for on-board digital processors

(ARTES-AT 5C.443 – 2 M€)

UDSM 1 — Started

UDSM Foundation and Platform Technology

(GSTP EEE GTE3-101ED – 19 M€)

UDSM 2 — ITT Preparation

UDSM Interface and System-in-Package Technology

(GSTP EEE GTE3-102ED – 20 M€)

UDSM HSSL — ITT Preparation

UDSM SERDES IP CORE

(GSTP EEE GTE3-103ED – 2 M€)

UDSM RF IP

Converters for telecom beamforming

foreseen

European Supply chain for UDSM ICs

Rad-Hard Design Libraries

IP Cores

Technologies:
FDSOI 22 nm
FinFET 7 nm

UDSM 3: GPP

UDSM General Purpose Processor SoC including eFPGA

foreseen

UDSM 4: FPGA

UDSM FPGA Soc including processor cores

foreseen

UDSM RF

UDSM Beamforming SoC

foreseen

Development Plan – Generic Components

- **Foundation and Platform Technology – GTE3-101ED (HI Approach)**
  - Develop GPP Prototype Testchip/Chiplet
  - GPP Component Prime
  - Supported by IP Companies
  - Develop
    - Foundation Library IP
    - Interfaces IP
    - Back-end Services
    - Heterogeneous Integration

- **Interface and System in Package Technology – GTE3-102ED (SoC Approach)**
  - Develop FPGA Prototype Testchip/Chiplet
  - Component Prime
  - Supported by
    - Application Product Companies
    - IP Companies
  - Develop
    - Interfaces and Controller IP
    - Application Prototype

Objectives

Ultra Deep Sub-Micron

GPP

GTE3-101ED - Foundation and Platform Technology

19ME – Kick Off: 15 Nov 2024

Description :

FDSOI STM 28nm

- Die to die interface in 28nm – (CNRZ and/or UCIe)

FDSOI GF 22nm

- Foundation library
- Die to die interface in 22nm – (CNRZ and/or UCIe)
- HSSL SR and LR 28G
- DDR4
- PCIe, Ethernet, SpF controller
- **Router 28G**

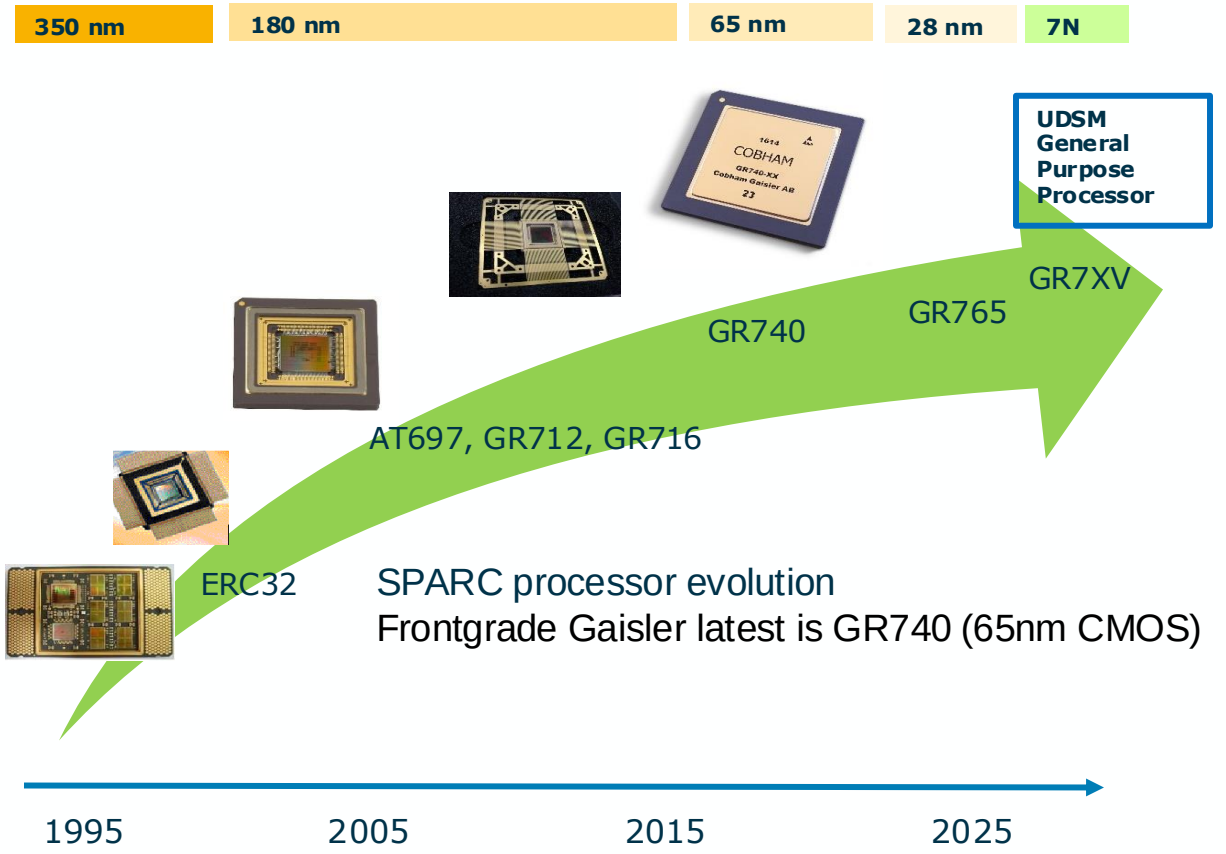
FinFET TSMC N7

- Foundation library
- **RISC-V Chiplet**

TO: B. Glass

Objectives: General Purpose Processor:

- Develop next generation European space general purpose processor, based on open-source RISC-V and exploiting N7 FinFET technology
- Develop a mature SW tool ecosystem to exploit multi-core parallel processing



Status

Ultra Deep Sub-Micron

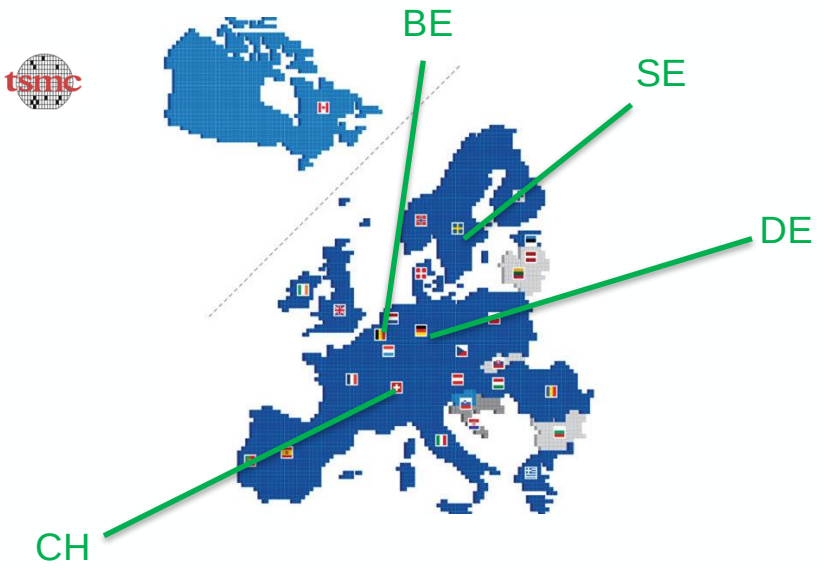
GTE3-101ED - Foundation and Platform Technology

19ME – Under evaluation

Status: Negotiation finished, Kick off on November 15, 2024

Challenges:

- ❑ Alignment with GTE-102ED



TO: B. Glass

Objectives

Ultra Deep Sub-Micron

FPGA

GTE3-102ED - Interface and System-in-Package Technology

20ME – Under preparation

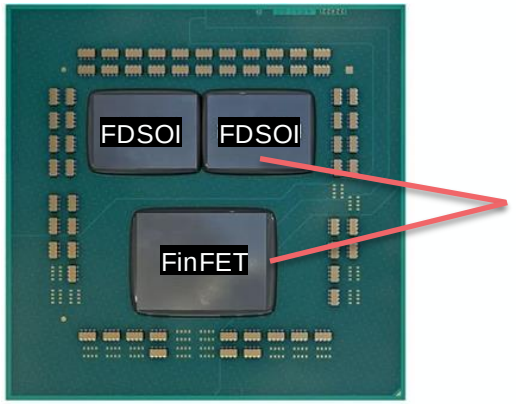
Description :

Contribute to the FPGA Development Roadmap

FinFET TSMC N7

- ❑ Foundation library
- ❑ Die to die interface in 7nm
- ❑ HSSL LR 112G
- ❑ PCIe, Ethernet and SpF controller
- ❑ DDR4
- ❑ **FPGA/DSA chiplet**

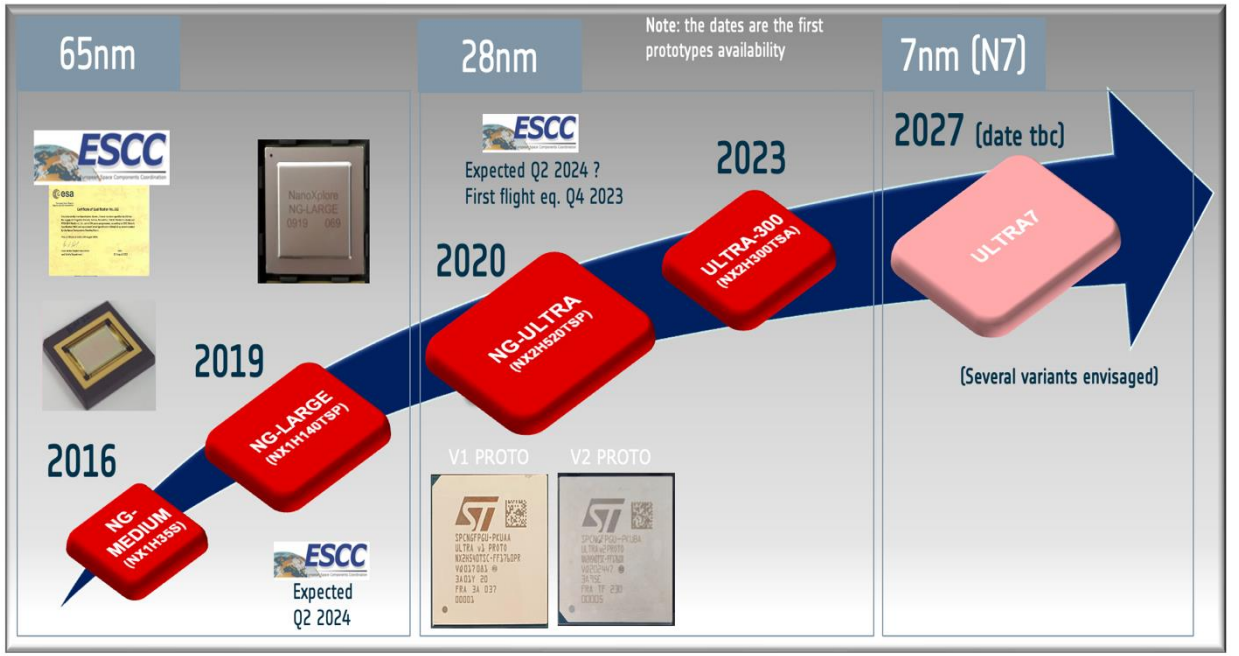
SiP Technology



Chiplets

Roadmap: Field Programmable Gate Array (FPGA):

- ❑ Increase portfolio of European FPGAs (RF and security)
- ❑ Develop next generation FPGA ULTRA 7
- ❑ Mature FPGA development tools



Status

Ultra Deep Sub-Micron

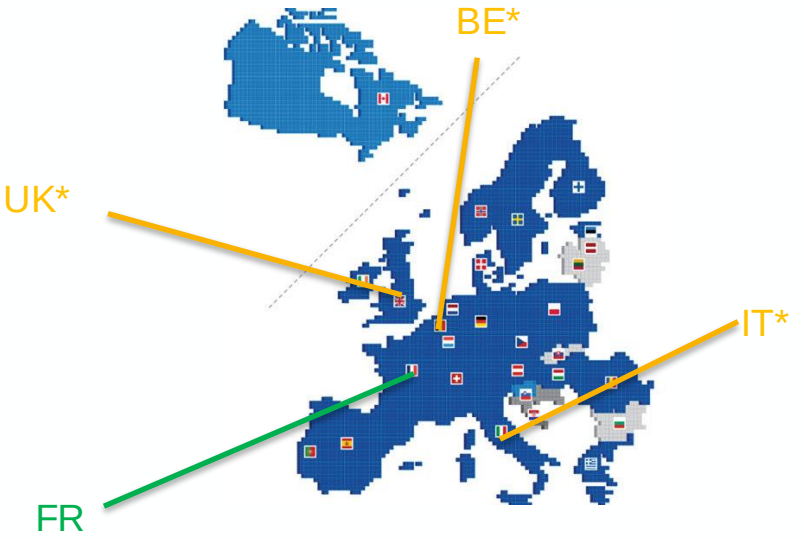
GTE3-102ED - Interface and System-in-Package Technology

20ME – Under preparation

Status: ITT in preparation, seeking for delegate support

Challenges:

- ❑ Aligning IP specification
- ❑ IP cross licensing of building block IP
- ❑ Testchip manufacturing



* Interest confirmed, support to be provided

TO: D. Merodio

Status EEE Component Sovereignty Initiative

- **Foundation and Platform Technology – GTE3-101ED – 19 M€**
  - Technical Requirements Specification Determined
  - Work package content defined
  - ITT released – Q2 2024
  - Negotiation Successful – Q4 2024
  - Activity KO – Q4 2024
  - Consortium
    - Frontgrade Gaisler (SE)
    - IMEC (BE)
    - IMST (DE)

Signing of Contract – 11/12/2024

GTE3-101ED

- **Interface and System in Package Technology – GTE3-102ED – 20 M€**
  - Delegate support received: BE, FR, IT (expected), UK
  - Technical Requirements Specification Determined
  - Work package content under review (with inclusion of additional UDSM products pre-developments)
  - ITT to be released – Q2 2025

GTE3-102ED

UDSM Component Product Portfolio

Field Programmable Gate Array (FPGA):

- Increase portfolio of European FPGAs (RF and security)
- Develop next generation FPGA ULTRA 7
- Mature FPGA development tools

General Purpose Processor (GPP)

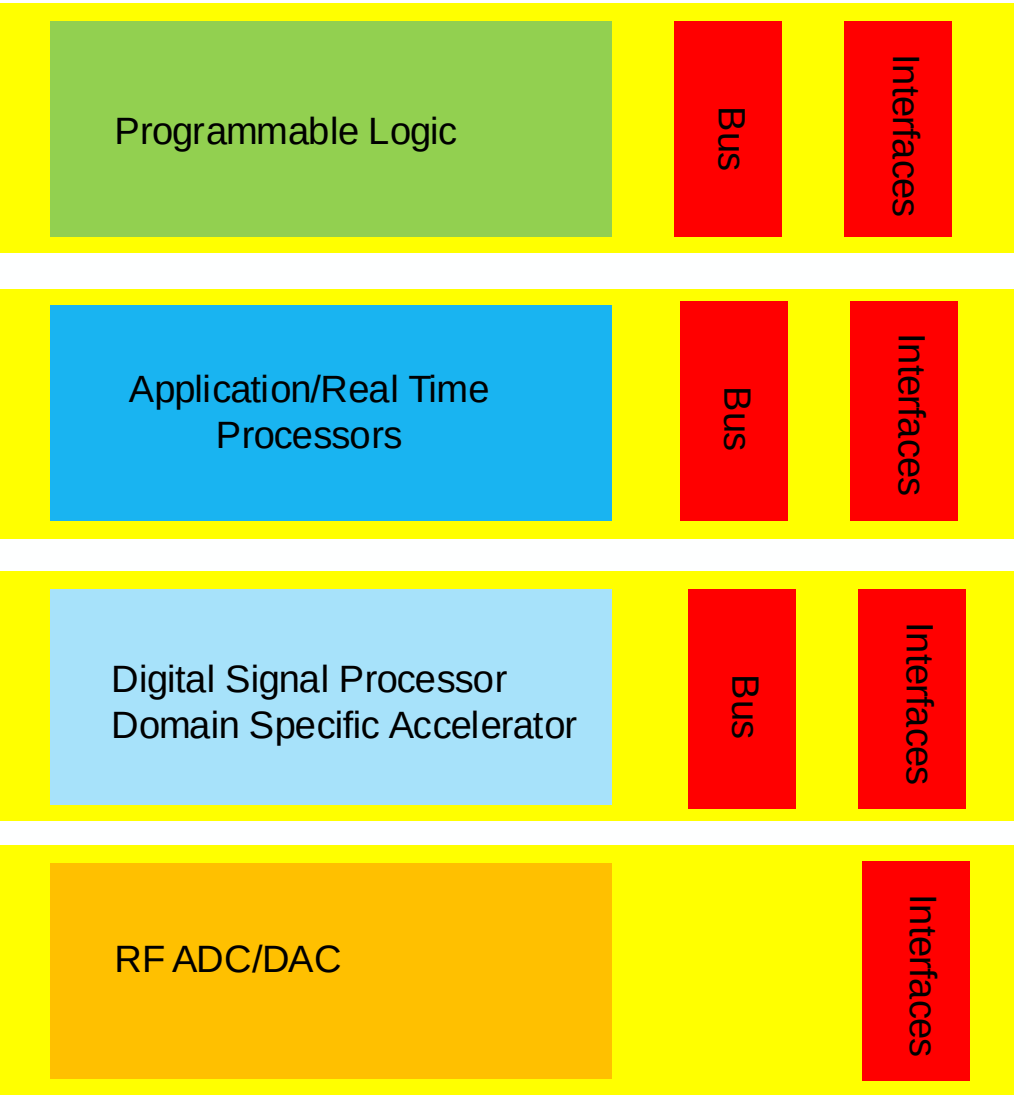
- Develop next generation European space general purpose processor, based on open-source RISC-V and exploiting N7 FinFET technology
- Develop a mature SW tool ecosystem to exploit multi-core parallel processing

General Purpose Accelerator (GPA)

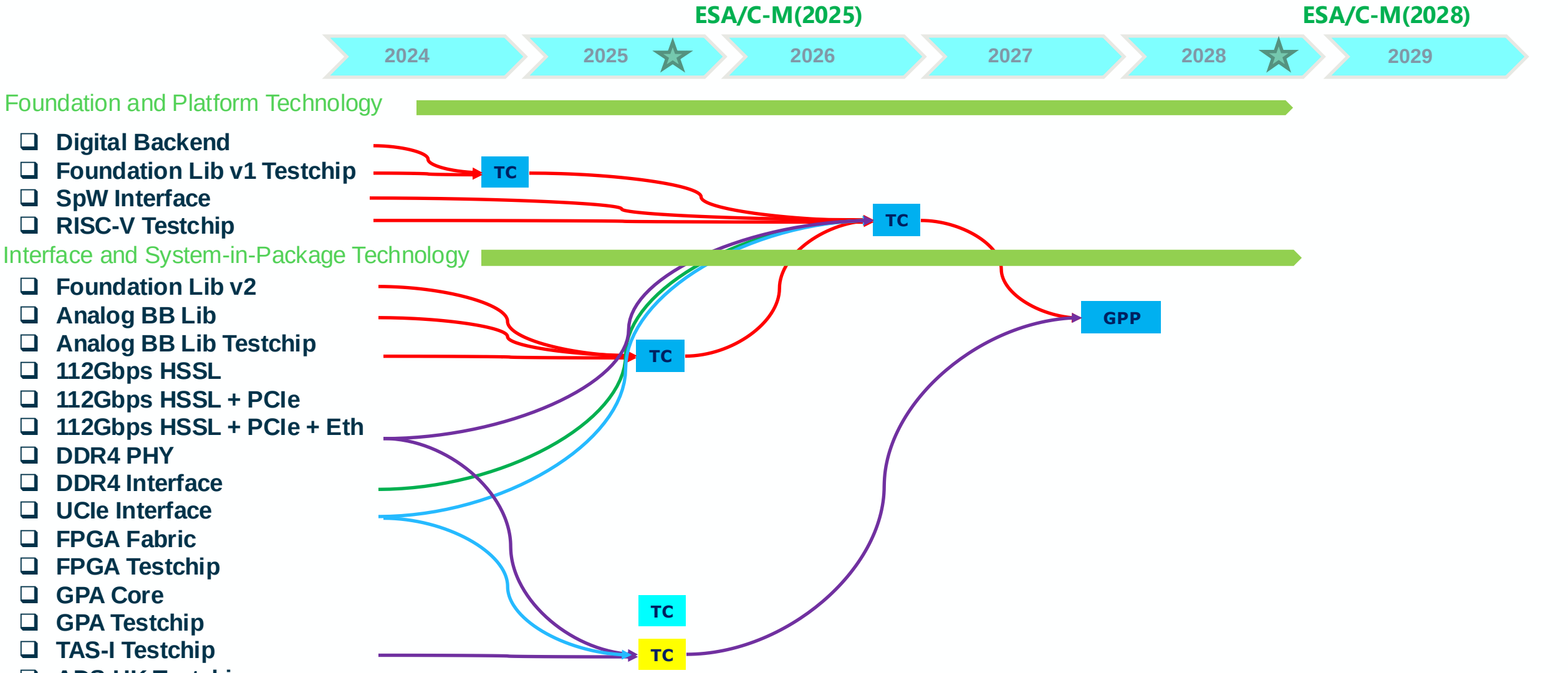
- Develop high performance European space general purpose accelerator, based on open-source RISC-V and exploiting N7 FinFET technology
- Applications: Digital Signal Processing for SAR, Digital Beamforming, AI,
- Develop a mature SW tool ecosystem to exploit multi-core parallel processing

Digital Beamforming (DBF)

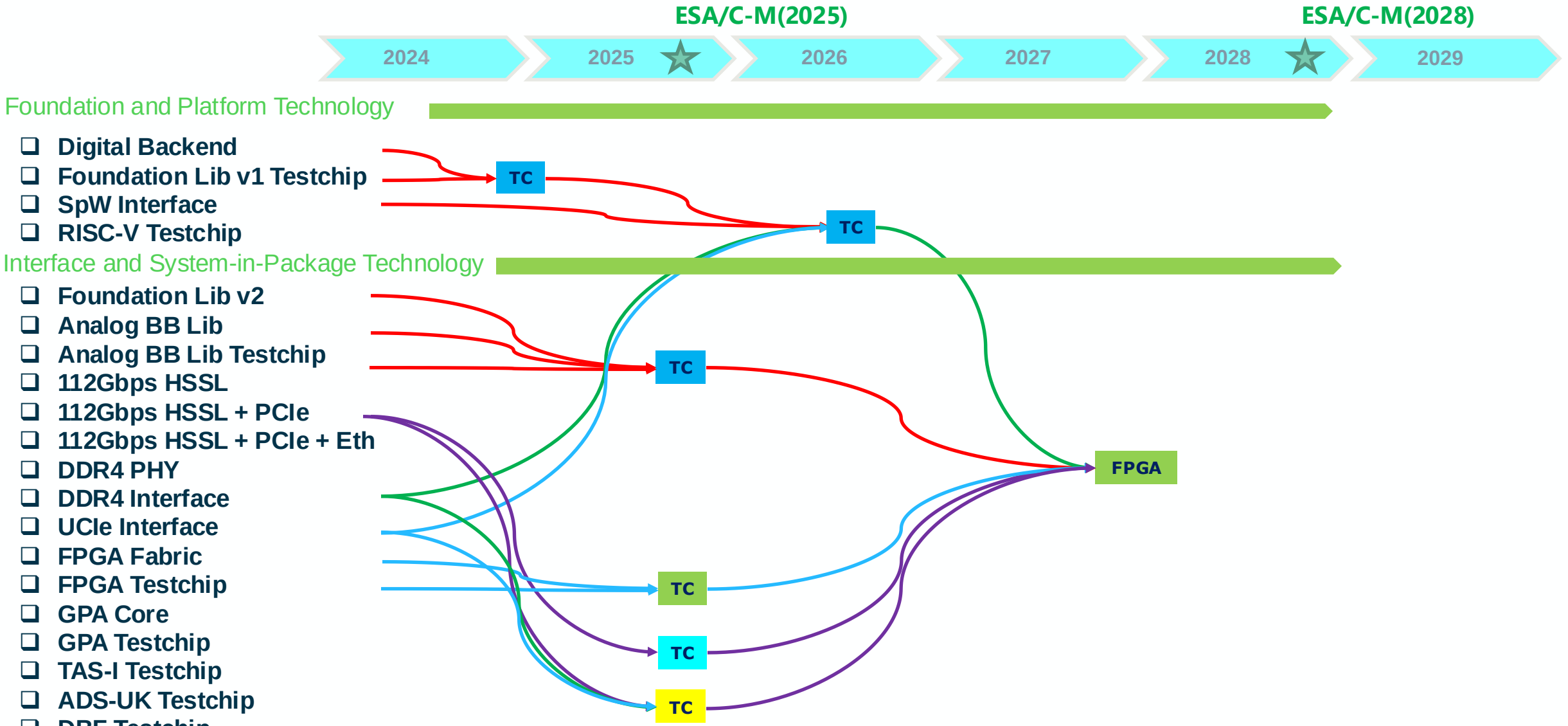
- Develop antenna digital beamforming chipset based on N7 FinFET technology
- Develop low-power ADC/DAC on N7 FinFET technology
- Develop a digital beamforming processor



UDSM N7 Development Plan - GPP



UDSM N7 Development Plan - FPGA



Extension UDSM Technology and IP

By extending the range of IPs the UDSM technology could also become of interest to specific payload applications.

The proposed IPs are:

- General Purpose Accelerator (RISC-V based)
- High Speed Serial Link (Short Range) PHY
- RF ADC and DAC
- High Speed Digital Down Conversion
- System in Package with optical interconnect

Two WG are working to determine the requirements for these payload applications

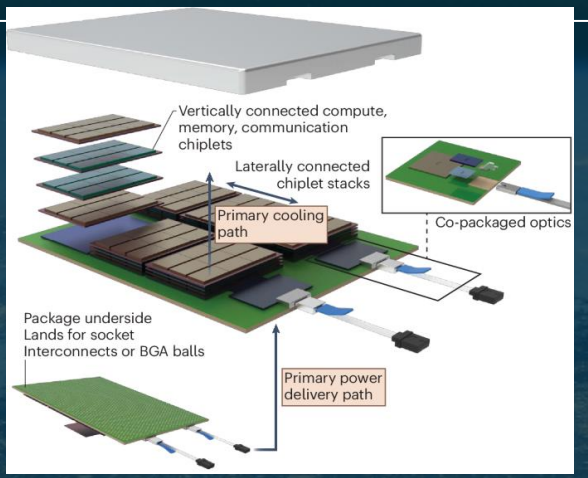
- Beamforming WG
- UDSM Processor WG

Specifically for telecommunication processors a 3rd working is proposed to be started

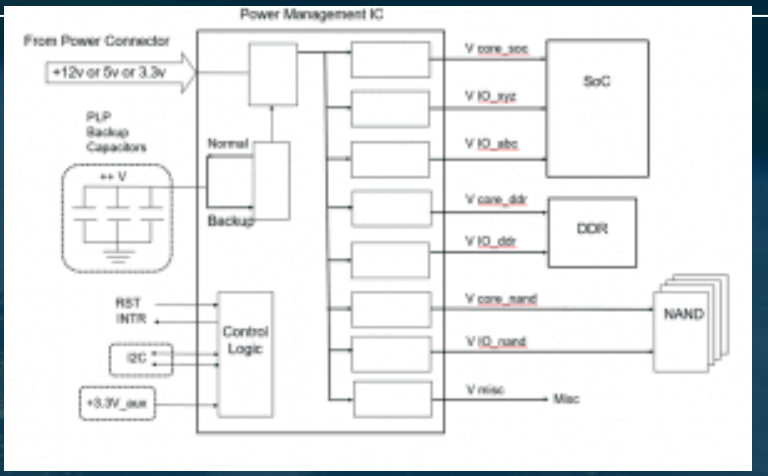
- Tele-communication Processor WG

Complementary Technology Developments

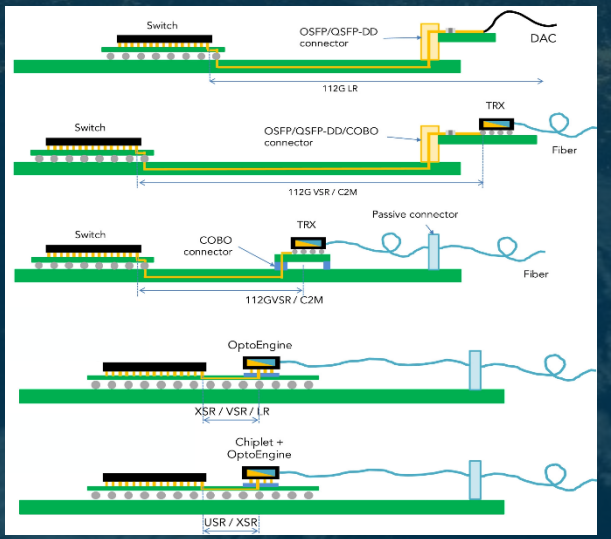
- Parallel Computing Technology
- Embedded Computing Technology
- Memory Technology
  - Volatile
  - Non-volatile Memory
- Power Management Technology
- Digital Interfacing Technology
  - Electrical Transceivers
  - Optical Transceivers
  - Routers/Switches/Retimers
- Converter Technology
- System in Package Technology
  - 2D and 2.5D
- Digital IP (Security, Comms, AI, Interfacing, …)



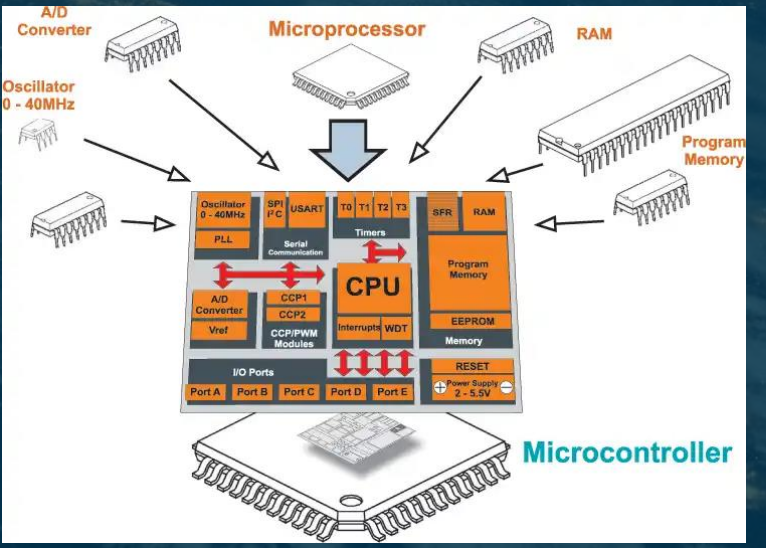
Digital Interfacing Technology



Power Management Technology – Power Management IC



Digital Interfacing Technology – Optical Transceivers



Embedded Computing Technology - Microcontroller

Thank you

Analogue and Mixed Signal ASICs for Space

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