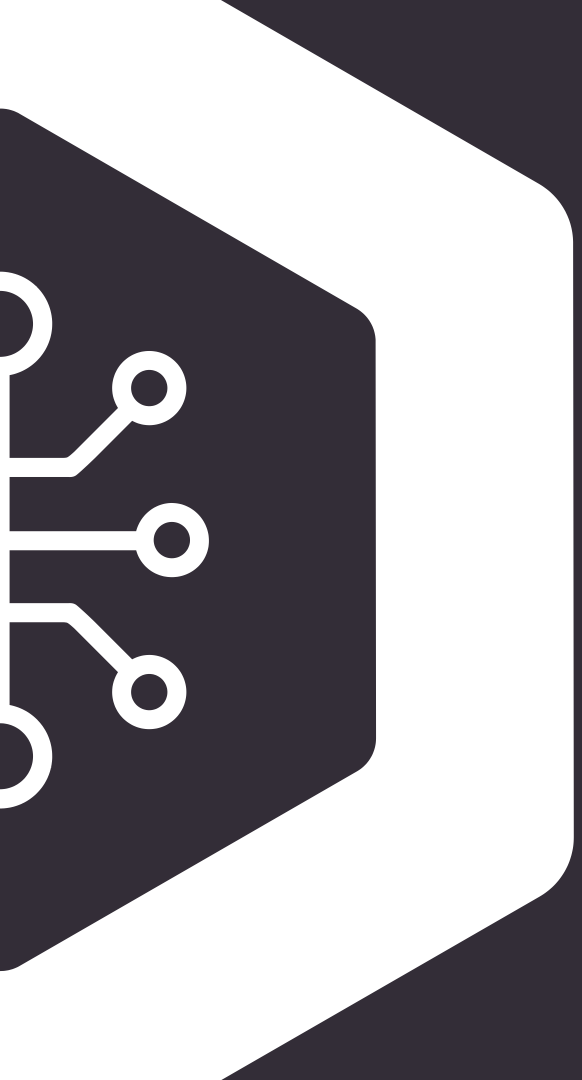

Develop your next RISC-V based spacecraft with a digital twin in Renode

RISC-V in Space, Gothenburg, 2025-04-02

Piotr Zierhoffer, pzierhoffer@antmicro.com

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Antmicro

- Founded in 2009
- Working on ASICs, HW, SW, FPGA, AI, simulation and much more
- Providing end-to-end engineering services, software/hardware co-design, advanced tooling development and strategic R&D for building high-tech products
- Founding member of RISC-V International, CHIPS Alliance
- Maintaining RISC-V in Zephyr RTOS
- Building commercially supported open source tools and platforms solving common problems

Develop your next RISC-V based spacecraft with a digital twin in Renode

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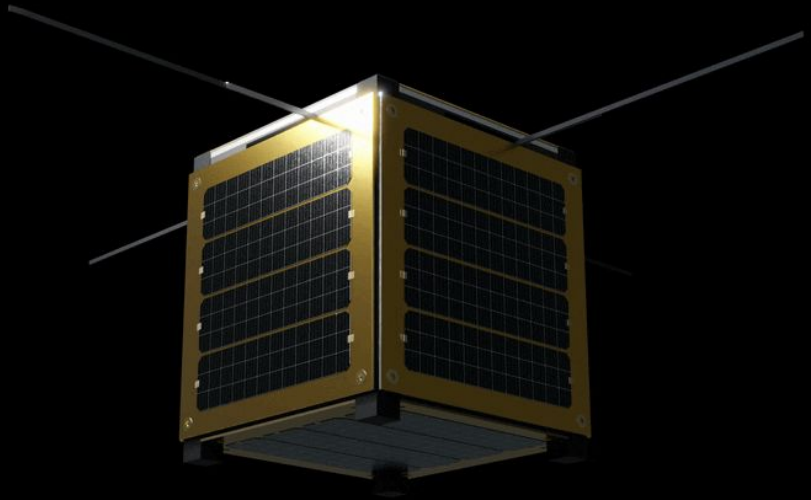

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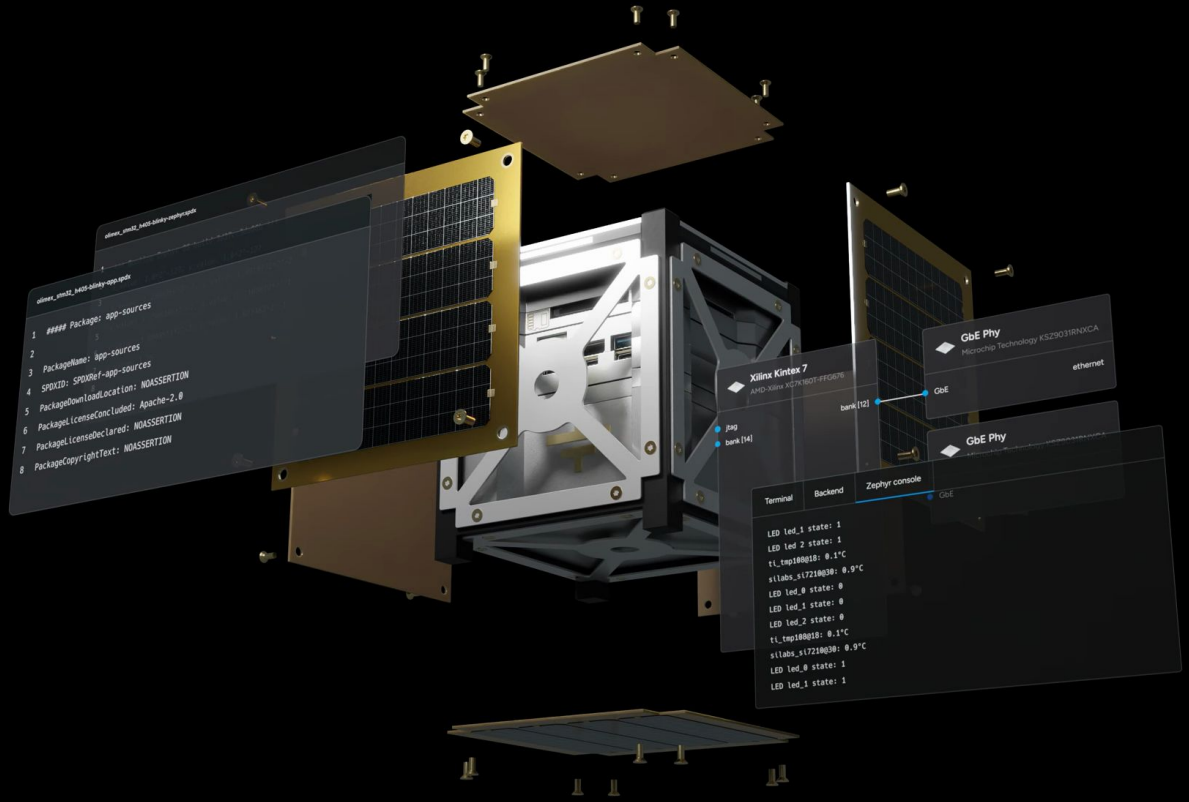

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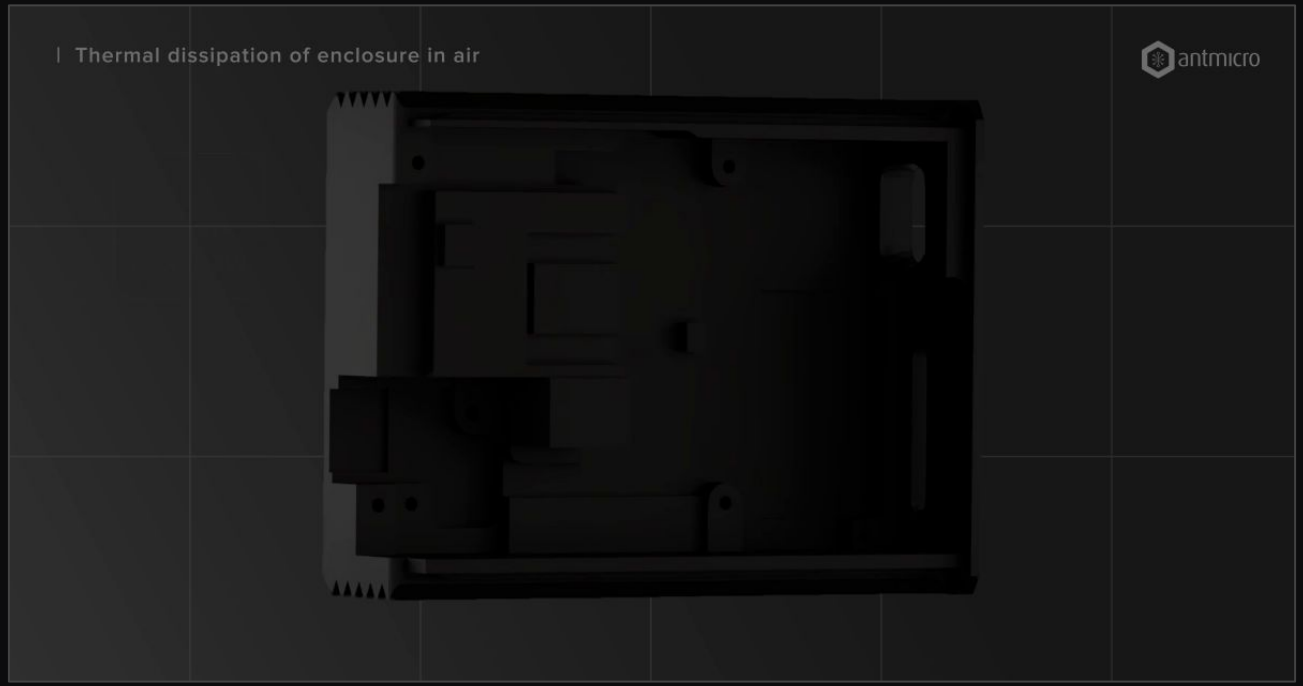

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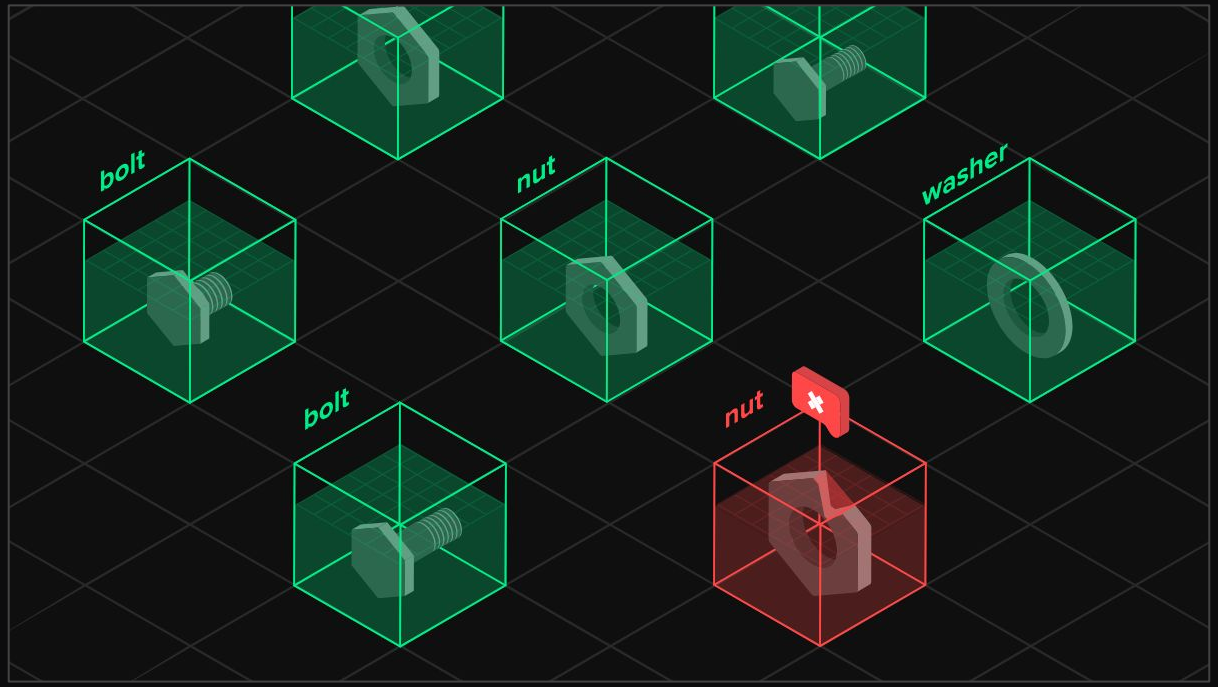

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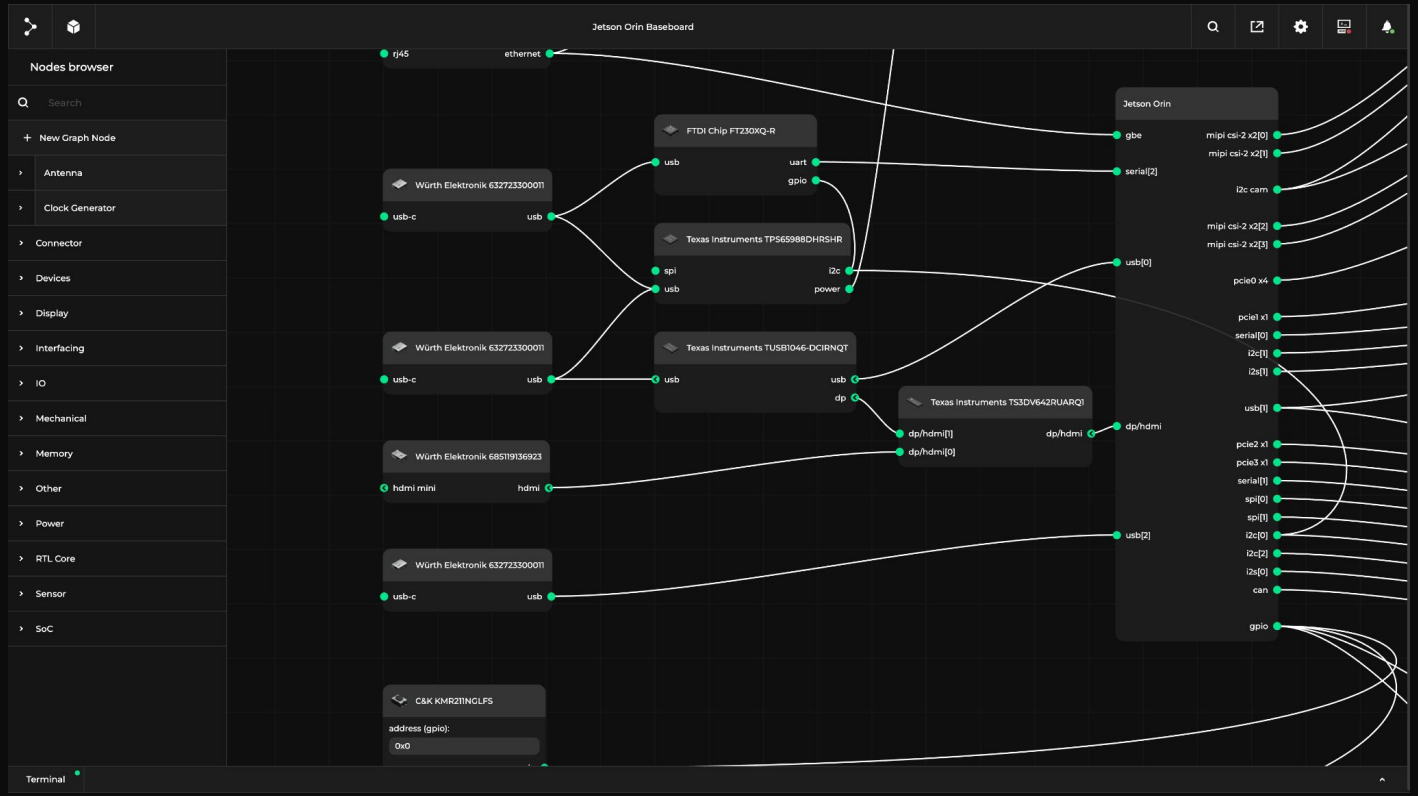
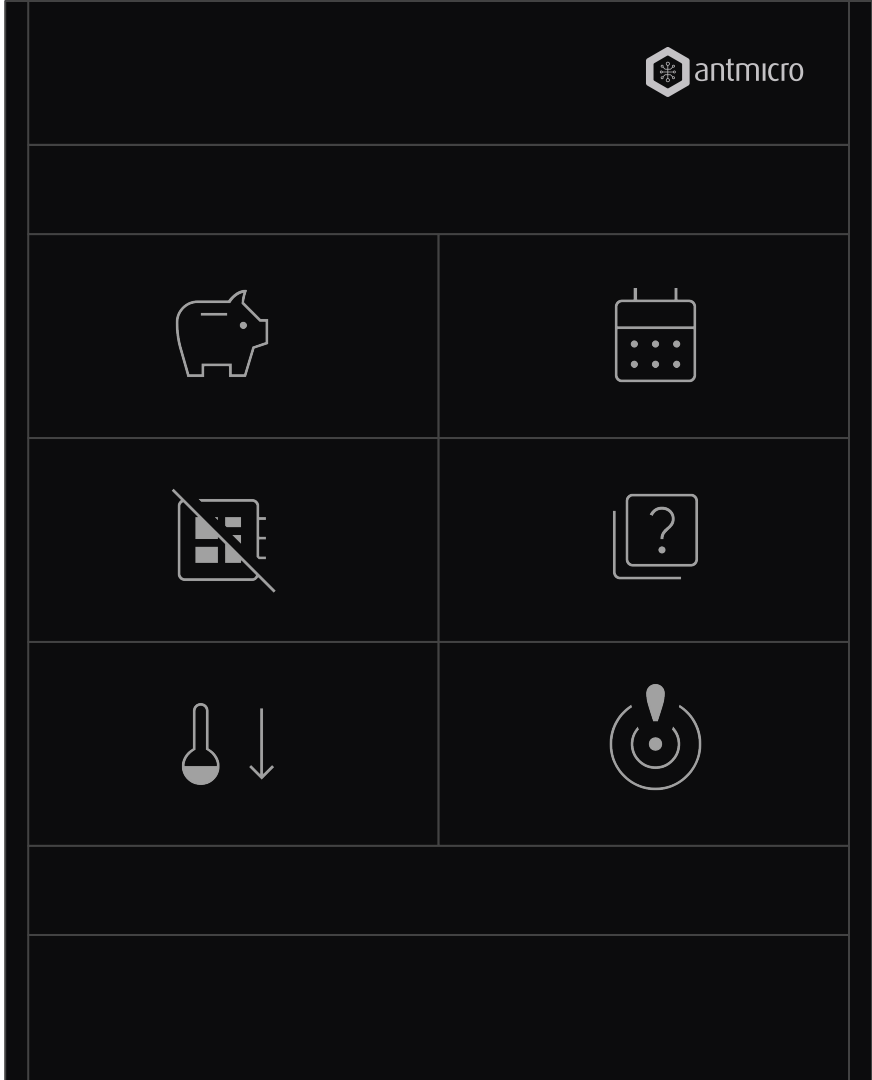


Development for space is hard

- High stakes, high costs
- Specialized hardware often long in the making
- Testing SW on the whole hardware setup is often impractical
  - It's difficult to give each engineer their own satellite for tests
- Virtually impossible to test real operating conditions



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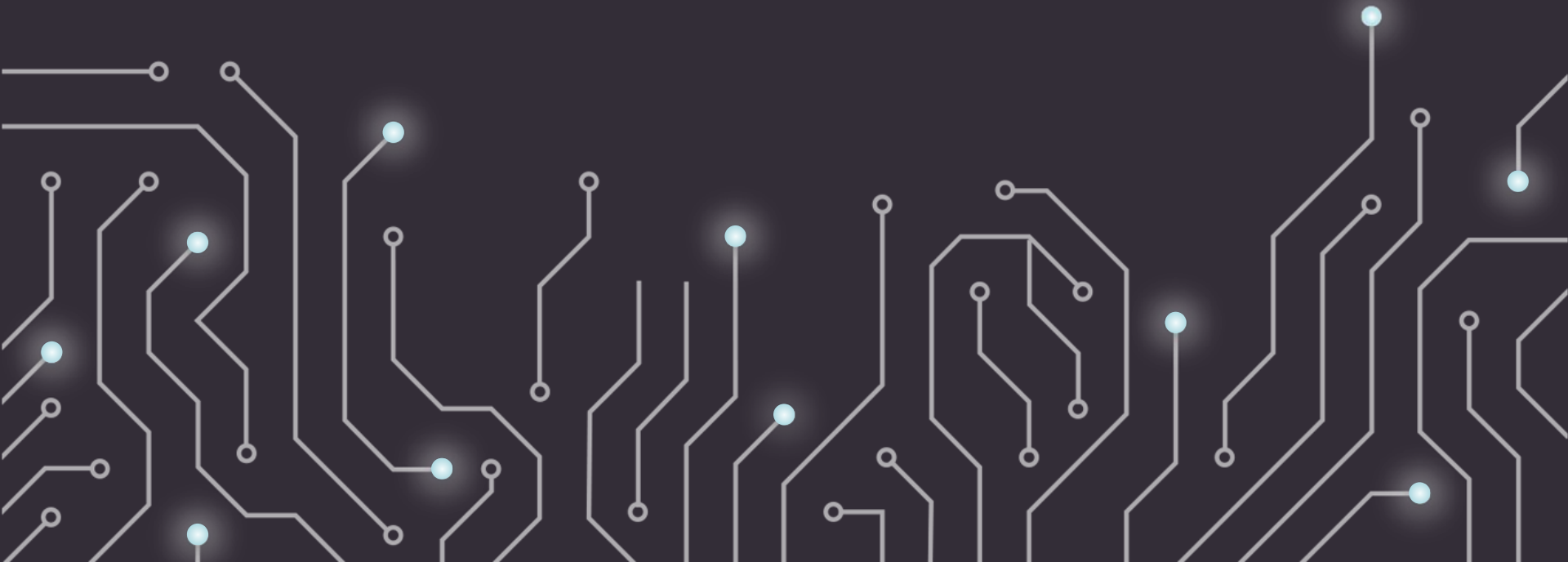
Digital Twins with Renode



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Renode

- Full system simulator
- Run the same binaries you'd run on hardware
- Prepare multi-node setups with various connectivity options
- Simulate sensor input
- Fully open source, permissively licensed

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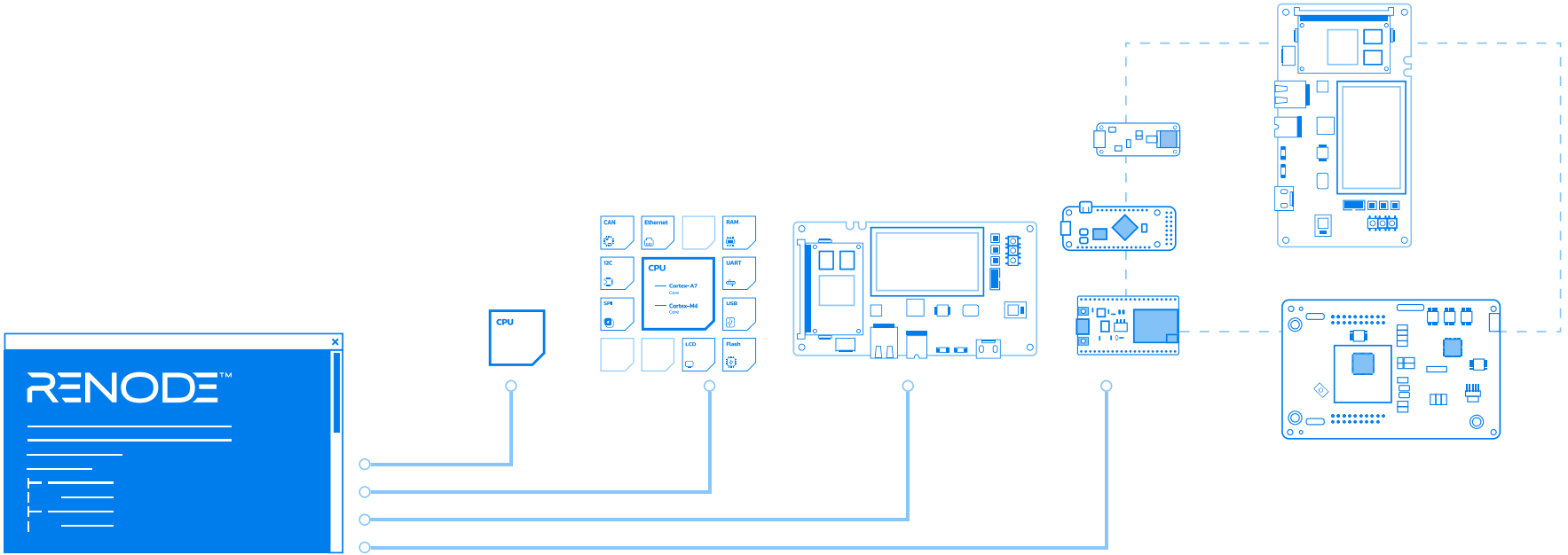
Simulate systems on different levels



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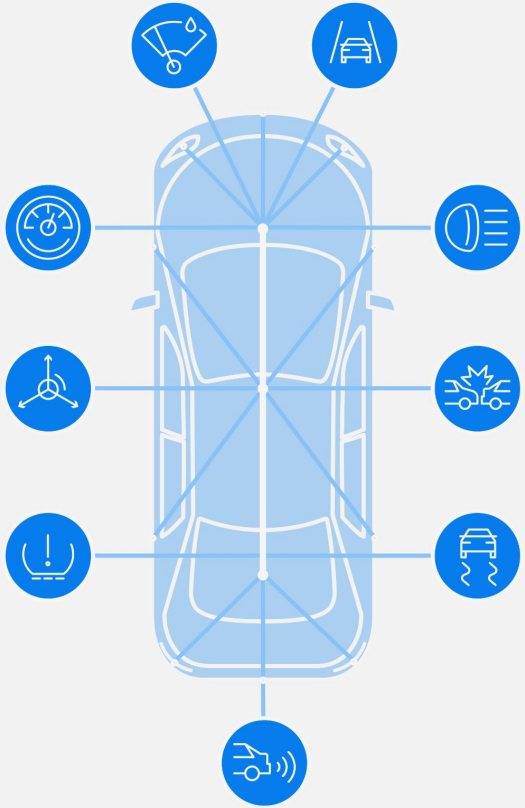
Full system simulation

- No "Renode" compilation targets
- Run exactly the same software you'd run on hardware
- Include complex boot flow or cut corners if you feel like it
- Test the whole stack in one go
  - business logic
  - communication protocols
  - drivers



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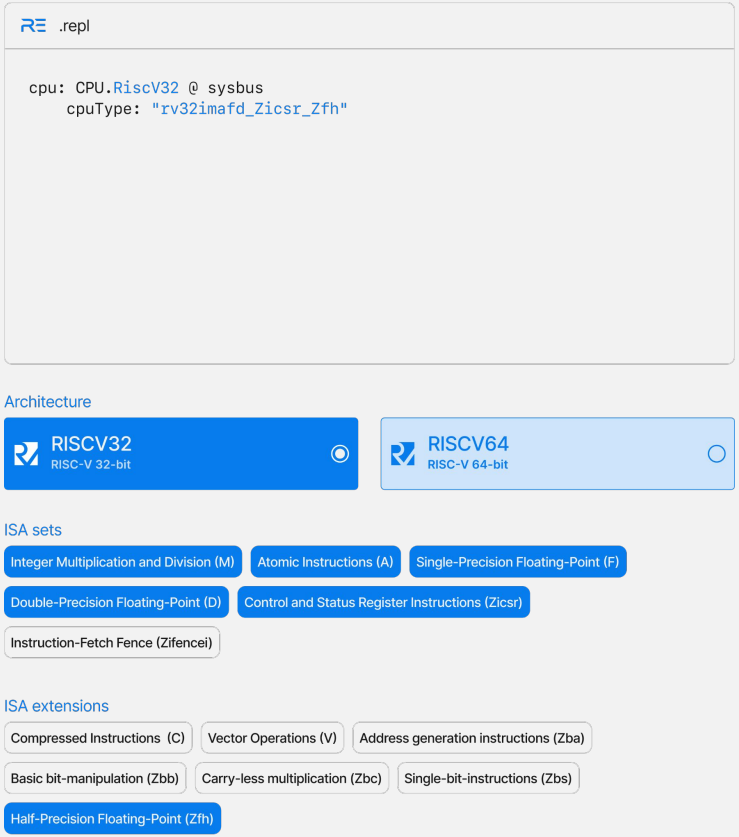
Heterogeneous systems support

- Range of ISAs supported
  - Arm Cortex-A/R/M
  - RISC-V with a wide range of extensions
    - easily define your custom extensions as well
  - POWER, SPARC, MSP430
  - ...
- Multi-core and multi-node setups, various connectivity options
- Determinism of execution even in multi-node systems



Understand your system

- Transparent GDB debugging
- Tracing and coverage reporting without code instrumentation
- Scriptable reactivity to various events

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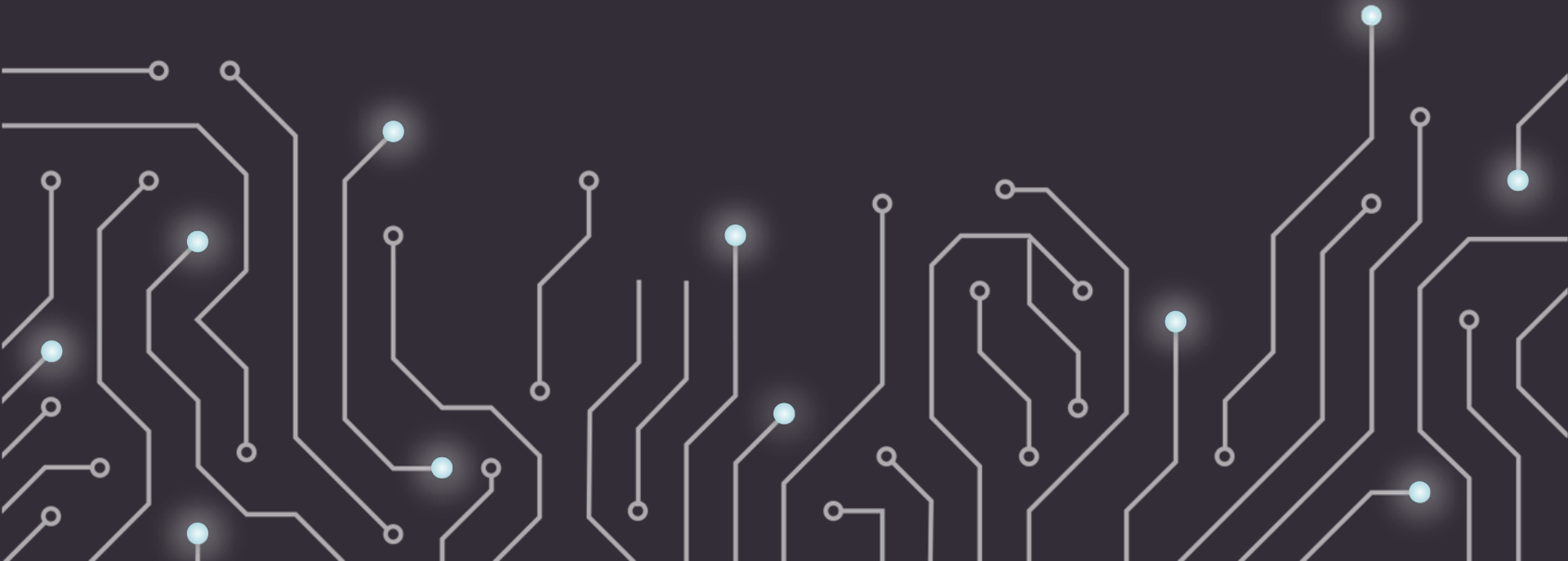
Renode and RISC-V



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Renode and RISC-V

- Collaboration with Microchip started in 2017
- Goal: support PolarFire SoC pre-silicon, also for their customers as part of the SoftConsole IDE
- Since then:
  - broad support for standard extensions
  - vectors, bitmanip, half-precision floats
  - custom sets like Xandes or CV32E
  - user-defined instructions and CSRs
  - heavily tested in a range of projects

RENODE

RISC-V®

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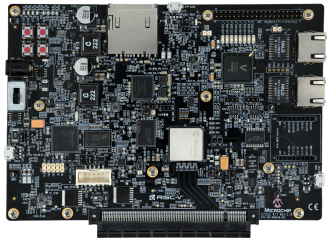
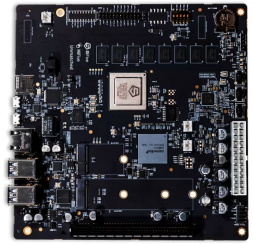
Broad platform support



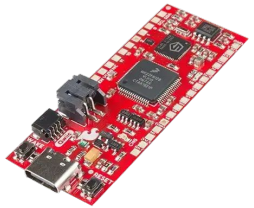
Microchip PolarFire SoC Icicle Kit



SiFive HiFive Unmatched

BeagleBoard BeagleV®-Fire

Andes Technology ADP-XC7K AE350



SparkFun RED-V Things Plus

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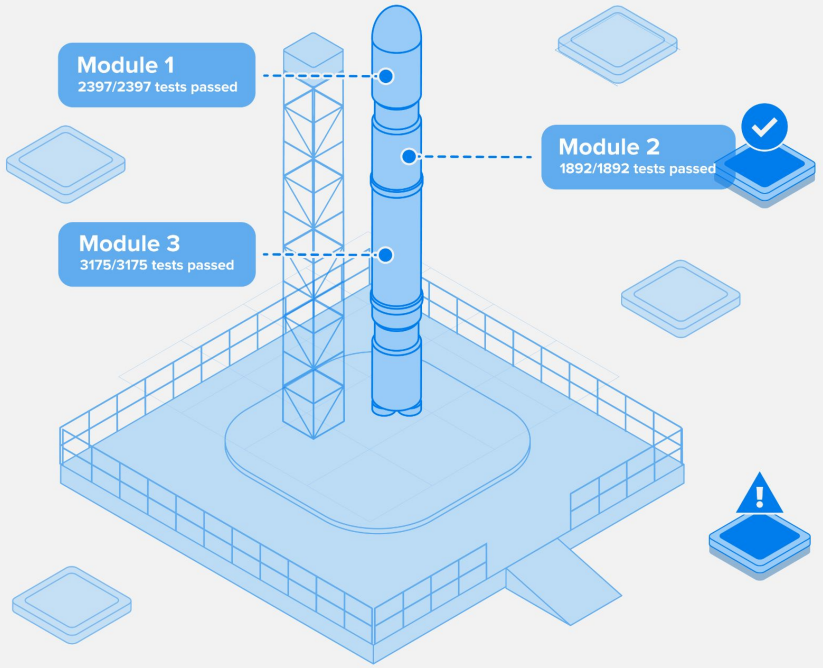
Send it to space

Complex development of space systems

- Peaking interest from the industry
- Various stages of development:
  - pre-silicon software development, closely following hardware
  - continuous testing of developed software
  - post-launch testing of OTA updates



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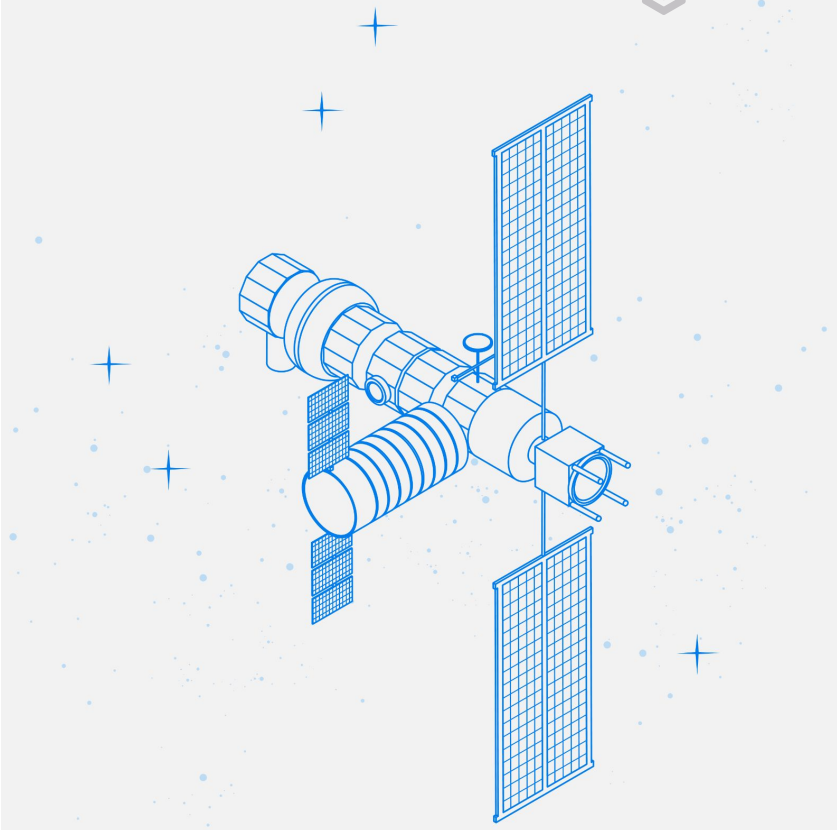
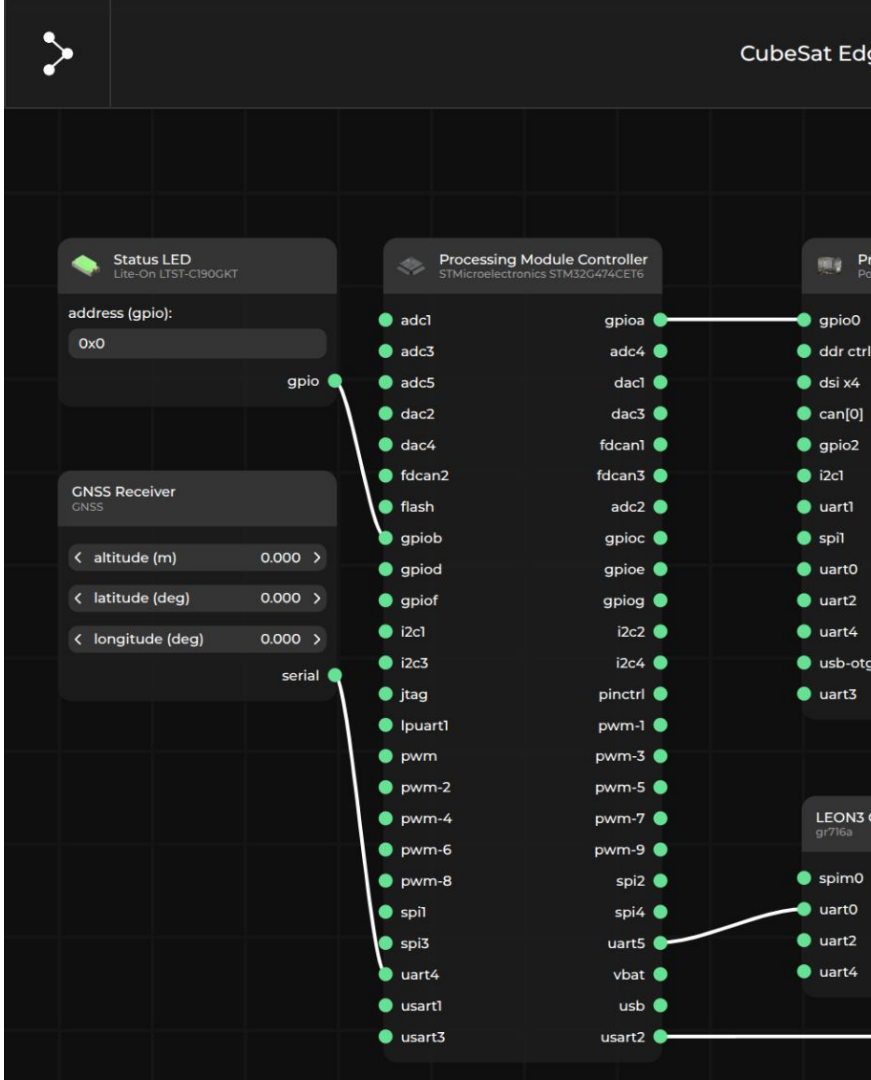
Feel like in space

- Renode can be easily integrated with external tooling
- Often used with aero/astrodynamics simulation tools
- Allows you to use tooling e.g. like Basilisk to feed sensors with test scenarios
- We can help integrate your tool of choice as well!



Handling complexity

- Renode is especially helpful with complex systems that span various functional blocks
- Simulate precisely what you care about
- Fast functional simulation for the main parts of the system
- Mock what is less important
- Co-simulate RTL for increased accuracy



REACH OUT TO LEARN MORE ABOUT RENODE!

contact@antmicro.com