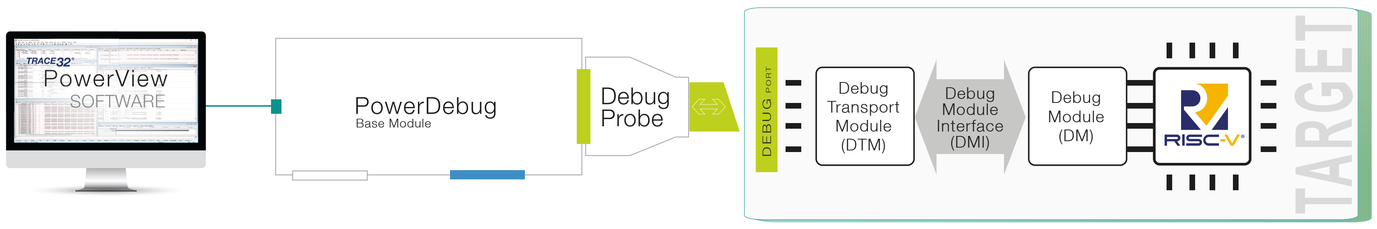
Heterogeneous Multicore Debugging of Space-Dedicated RISC-V Chips Made Easy

Introduction

RISC-V cores can be found in more and more space-dedicated chips – as the main CPU(s) or as a companion core together with other CPU architectures. They can be implemented in subarchitectures like RISC-V RV32/RV64, AndesCore™ V5 or SiFive® Core IP. While the complexity of SoCs grows with the number of cores and the number of different core (sub) architectures, the challenges for embedded developers in the space industry grow even more with operating systems, hypervisors, and other software running on multiple cores. The requirements for functional safety and security are also paramount.

Debug RISC-V SoCs

- „RISC-V External Debug Support“ Specification v1.0.0 incorporates everything needed for simple and complex debugging scenarios.
- Lauterbach was significant contributor to RISC-V Debug Specification.
- Great solution for simple and fairly complex RISC-V Systems
- Open to adaptions to support most complex and diverse SoCs
  - Flexible DTM designs make heterogeneous debugging easy
  - Several options to add peripheral IP such as Trace



LIVE-DEMO & DISCUSSION @ LAUTERBACH BOOTH

Lauterbach Supports All Space-Dedicated RISC-V SoCs

- Microchip PolarFire® SoC (all Series)
- Microchip PIC64 HPSC
- Frontgrade Gaisler NOEL-V

Trace RISC-V SoCs

- RISC-V trace specifications are also suitable for heterogeneous systems
- Flexible ways to access the trace component’s configuration registers via System Bus Access, DMI, …
- Filters to limit trace usage
- Transportability via other trace infrastructure such as CoreSight ATB
- Lauterbach supports the latest versions of the E- and N-Trace specifications in various implementations

TRACE BASED DEBUGGING

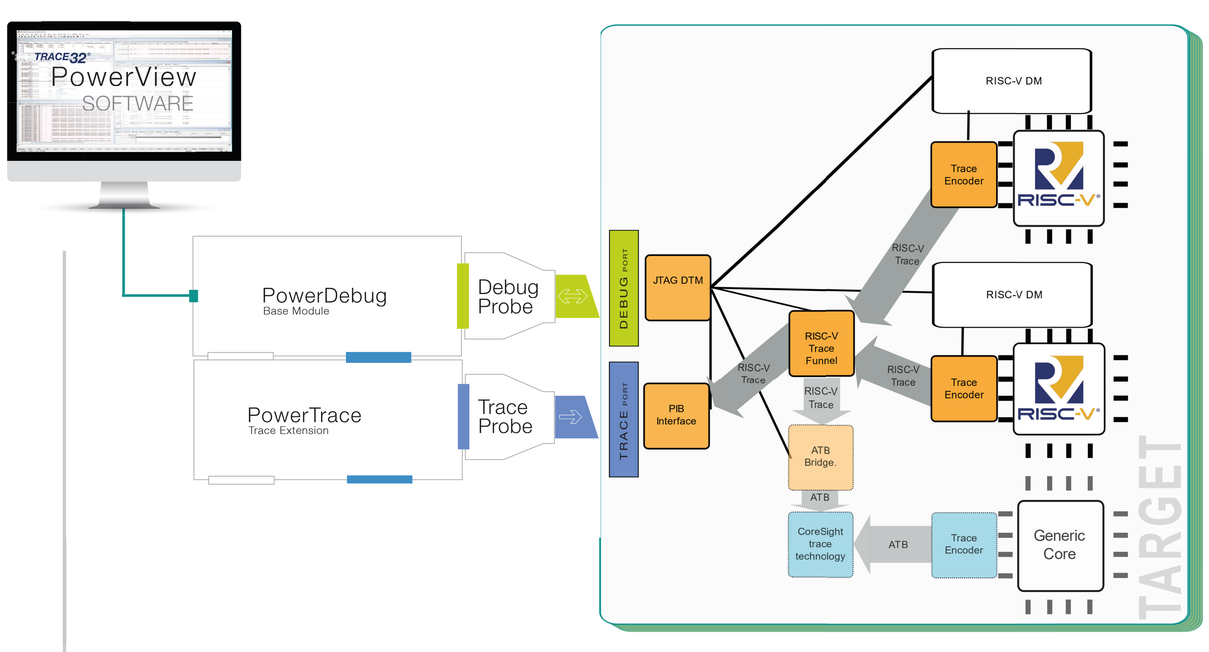
- Debug without stopping the CPU
- Find bugs which appear only in real time

OPTIMIZING WITH TIMING MEASUREMENTS

- Analyse the code performance of the application
- Analyse outside events

QUALIFICATION

- Prove the meeting of real time requirements
- Prove code coverage



N-TRACE	E-TRACE
Instruction Trace	Instruction + Data Trace
Inferable Jump Optimization	Inferable Jump Optimization
Implicit Return Optimization (in different modes)	Implicit Return Optimization
Repeated History Optimization	Address Optimization
Virtual Address Optimization	Implicit Exception Optimization
	Branch Prediction Optimization
	Jump Target Cache Optimization

RISC-V

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