SEE Characterization of NOEL-V on 28nm FD-SOI Platform for Space

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***Abstract*—This work presents the SEE characterization of the first Frontgrade Gaisler's NOEL-V implementation in a test chip. The device was built on STMicroelectronics' 28nm FD-SOI GEO P2 platform for Space. Results show the effectiveness of processor's fault tolerance in handling soft errors. All detected memory errors were successfully corrected without software interference.**

***Index Terms*— NOEL-VF, GR765, Heavy Ions, Protons, SEE, STM 28 nm FD-SOI.**

I. Introduction

THE NOEL-V is a state-of-the-art processor from Frontgrade Gaisler that implements the RISC-V architecture. The processor core features built-in Fault Tolerance (FT) and is part of the GRLIB Intellectual Property (IP) Library [1].

An Application Specific Integrated Circuit (ASIC) test chip, built on European STMicroelectronics' (STM) 28nm Fully Depleted Silicon-on-Insulator (FD-SOI) GEO P2 platform for Space, was developed as a collaboration between STMicroelectronics and Frontgrade Gaisler R&D teams. The test chip implements a NOEL-V core sharing resources with a LEON5 core (32-bit processor based on the SPARC V8 architecture) in a System-on-Chip (SoC) architecture.

This work aimed at the ground-level heavy ion and proton-induced Single Event Effects (SEE) testing of the ASIC test chip. Results show the high effectiveness of the NOEL-V fault tolerance features in dealing with memory errors, avoiding the error build-up.

This work was also motivated by the radiation characterization of the SoC fault tolerance features and technology to endorse the development of the GR765 [2], the next generation of high-performance space-grade SoC from Frontgrade Gaisler. The GR765 will be implemented using the STM 28 nm FD-SOI platform for Space and will feature an octa-core NOEL-V and LEON5 processor cluster.

II. STM 28nm FDSOI GEO P2 technology

STM 28nm FD-SOI GEO P2 platform for Space [3] is an extension of the P1 platform. It includes space-qualified analog IPs, such as but not limited to Low Voltage Differential Signaling (LVDS), Phase-Locked Loop (PLL), sensors, and more than 100 radiation-hardened sequential cells with several levels of Single Event Upset (SEU) robustness, power, performance, and area.

The libraries corners have been characterized to a Total Ionizing Dose (TID) of 50 krad(Si) as part of a space-grade signoff strategy. Guidelines are provided to ensure Single Event Transient (SET) mitigation in digital and/or custom analog circuits. The platform offers an intrinsic Single Event Latch-up (SEL) immunity in SOI areas. The P2 platform offers a new operating mode, enabling high speed, low power performances, using a lower supply voltage combined with Forward Body-Biasing (FBB).

III. NOEL-V processor

The NOEL-V [1] is a 64-bit RISC-V processor that can feature a dual-issue pipeline, enabling the parallel execution of up to two instructions per cycle, together with advanced branch prediction capability.

The cache memory of the NOEL-V processor core is safeguarded from radiation-induced SEUs through a custom patented error correction code (ECC) scheme [4]. The ECC scheme is part of the fault tolerance features of the NOEL-V processor. It can correct single-bit errors, detect double-bit errors, and even detect three- and four-bit adjacent errors. The one-bit error correction is implemented transparently in the cache controller without software intervention or extra memory access. The detected multiple-bit errors that cannot be handled directly by the ECC scheme are corrected at the system level through re-fetch from memory transparently to software. The cache also includes a hardware scrubber that can be activated to scrub the memories automatically, preventing error build-up.

IV. Device under test

The Device Under Test (DUT) is the ASIC test chip built to validate the NOEL-V fault tolerance functionalities. The DUT is manufactured on European technology, STM 28 nm FD-SOI GEO P2 platform, and packaged in a 304-pin Super Ball Grid Array (SBGA) cavity-down package.

The DUT features a single-core NOEL-V RISC-V 64-bit and a single-core LEON5FT SPARC V8 32-bit processors. The processor cores share the resources of the SoC, such as the cache memories, and cannot be enabled simultaneously. The SoC includes an 8 KB L1 cache, floating-point unit (FPU), 128 KB on-chip RAM (FTAHBRAM), SoC-bridge, GPIOs, and JTAG and UART interfaces. All IP cores are part of the GRLIB IP Library [1].

The test chip allows external control of its body bias: by tuning the body voltage from 0 to 1.1 V, the SoC can be adjusted to achieve low leakage or high performance. At high performance voltage conditions, the NOEL-V processor can

run up to 1 GHz.

V. SEE CHARACTERIZATION

A. Test hardware

A test board was built targeting the ground level SEE testing of the test chip with either heavy ions or protons. The DUT is placed into a socket, which facilitates the replacement of the part. The backside of the board has an opening to expose the DUT during irradiation. Fig. 1 shows the test board view.

The Test Controller (TC) is a Xilinx Artix-7 Field Programmable Gate Array (FPGA) module attached to the primary board. It controls the DUT and provides latch-up monitoring and protection capabilities. The TC FPGA and all active devices are placed at a distance from the DUT in order to not get irradiated during SEE testing.

The TC FPGA also controls the DUT's body bias and core voltage, allowing varying the power configuration during the test. Both NOEL-V and LEON5 processor cores were exercised at different bias conditions, as described in Table I.

B. Test software

Three test cases were used for the evaluation of both processor cores: IU (Integer Unit RAM test), that exercises all on-chip memories; Paranoia, to validate the floating-point unit; and Stanford, which is a set of benchmarks for general processor tests.

The test software suite was executed continuously looping all three test cases. The software contained self-checks that compared the results to expected values after execution in order to detect Silent Data Corruption (SDC) events. The reporting was performed via UART. The software was also capable of reporting detected and corrected errors in memory elements, such as the register file, L1 cache, and FTAHBRAM.

Single Event Functional Interrupt (SEFI) events were detected indirectly in log post-processing by detecting missing or corrupted progress messages from the DUT. A watchdog scheme was used to automatically allow the test controller to reboot the DUT in the event of a crash in order to not lose beam time, and such watchdog timeouts were also logged and time-stamped for post-processing and analysis. All messages from the DUT were logged with time stamps and post-processed offline on a host computer.

The GRMON3 software [5] was used on the host computer to monitor the complete test system through Ethernet communication with the TC FPGA.

C. Heavy ion testing

The Heavy Ion (HI) test campaign was performed at the Heavy Ion Facility (HIF) at the Université Catholique de Louvain (UCL), Belgium. The irradiation was in vacuum using an ion cocktail covering the full Linear Energy Transfer (LET) range from 1.3 to 91.9 MeV/mg/cm^2 at room temperature. The DUT was irradiated at a normal incidence angle and tilted at 45° to reach higher LETs. The DUT test sample was de-capsulated, allowing heavy ions over the full LET range to reach the sensitive region of the die. The target fluence per run was up to 5×10^7 ions/cm^2, with an average flux of 1×10^4 ions/cm^2/s. The DUT accumulated a TID of about 44 krad(Si).

D. Proton testing

The proton test campaign was performed at the Proton Irradiation Facility (PIF) at the Paul Scherrer Institut (PSI), Switzerland. A different test sample from the HI campaign, without preparation, was used for the proton testing. The irradiation was in air using the following proton energies: 23.5, 101.3, and 230 MeV. The DUT was irradiated at a normal incidence angle at room temperature. A collimator with dimensions of 18×18 mm was set the closest possible to the DUT to avoid the high spread of particles affecting other components on the board. The target fluence per run was up to 1×10^{11} p/cm^2, with an average flux of 1×10^8 p/cm^2/s. The accumulated TID was of about 117 krad(Si). The proton beam time was granted by the RADNEXT project [7].

E. Test conditions

Both NOEL-V and LEON5 processors were validated during the heavy ion and proton testing. Table I describes the different configurations tested. The factors differ between the selected processor core, frequency, and core (VCORE) and body bias (VBODY) voltage. During the proton testing, there was the opportunity to exercise more DUT conditions and test at different configurations.

VI. RESULTS

A. Heavy ions

All detected errors in the L1 cache and FTAHBRAM memories were successfully corrected. The test software had no execution interference since the processor fault tolerance features handled those errors. Fig. 2 depicts the total correctable errors cross-section per bit (arbitrary unit) for both processors obtained for the L1 cache and FTAHBRAM memories. The results match the ones reported for the technology in [4].

No test case SDC was reported on either processor at any LET. No functional event was observed for the NOEL-V. Four functional events in total were observed for the LEON5 processor during the entire test campaign. The root cause of these events is believed to be a test artifact due to the high flux of ions used during testing. The test software logging provided low traceability of the functional events, which could not be reproducible during emulation testing. The test software was enhanced before the proton testing for better visibility in case of any events. A conservative approach is taken to consider the functional events in the error rate analysis, as described in

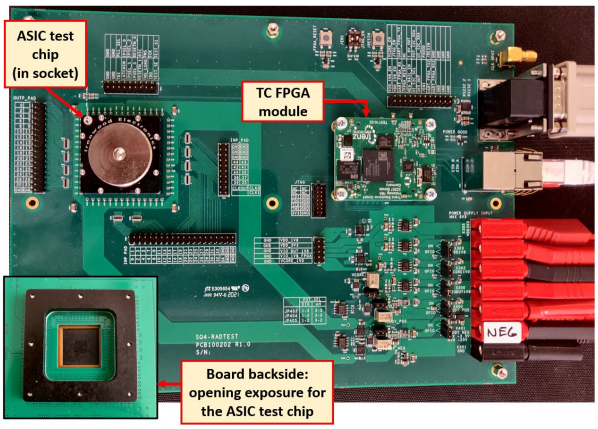

Fig. 1. Test board view.

TABLE I
DUT BIAS AND FREQUENCY CONDITIONS DURING SEE TESTING.
NV = NOEL-V, L5 = LEON5.

SEE testing	Condition	Frequency (MHz)	VCORE (mV)	VBODY (mV)
HI	NV-LF	250	670	1100
HI	NV-HI	400	1100	1100
HI / Protons	L5-HI	500	1100	1100
HI / Protons	L5-GX	500	900	0
Protons	NV-GX	400	900	0
Protons	NV/L5-HP1	1000	1100	1100
Protons	L5-HP2	1000	900	1100
Protons	NV/L5-LP	250	670	0
Protons	L5-TID	100	1100	0

section VI-C. No SEL was observed at any LET at nominal supplies and room temperature.

B. *Protons*

Fig. 3 shows the total correctable error cross-section per bit (arbitrary unit) of the embedded memories obtained during proton testing for NOEL-V and LEON5. Similarly to the previous heavy ions results, all detected errors in the L1 cache and FTAHBRAM memories were corrected, and the data matches the technology's expectations [4]. As described in Table I, the processors were tested at different frequency and bias conditions. From the results, one can notice that reducing the DUT core voltage has a high influence on the memory cross-section. As expected, reducing the core voltage increases the SEU susceptibility [8].

No test case SDC, functional event, or SEL was observed at any proton energy or DUT condition, which strengthens the argument of test artefact during heavy ion testing.

C. *SEE rates in orbit*

Low Earth Orbit (LEO - 700 km, 98.7° inclination) and Geostationary orbit (GEO - 36000 km) were evaluated using CREME96 with Z =1-92 for heavy ions and AP8min for protons, with 1 g/cm^2 of Al shielding.

Table II describes the mean time between events per orbit for L1 cache and FTAHBRAM correctable errors, and functional events, considering both heavy ion and proton testing for the LEON5 processor (worst-case approach). It is worth highlighting that the memory correctable errors are handled by the processor's fault tolerance features and do not contribute to any functional event in the system.

TABLE II
MEAN TIME BETWEEN EVENTS

Orbit	L1 cache correctable errors	FTAHBRAM correctable errors	Functional events
LEO	1,030 days	197 days	28,500 years
GEO	787 days	141 days	8,640 years

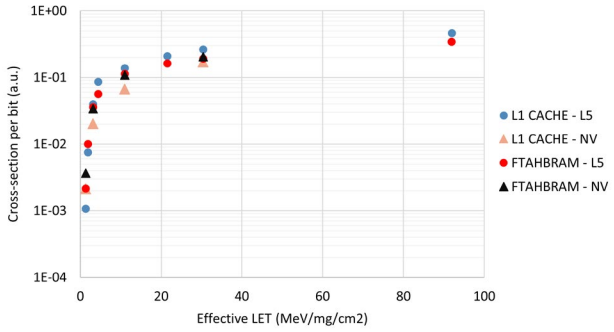

Fig. 2. Total correctable errors cross-section per bit (arbitrary unit) for L1 cache and FTAHBRAM memories of NOEL-V and LEON5 processors during HI testing. The presented data is for combined test conditions.

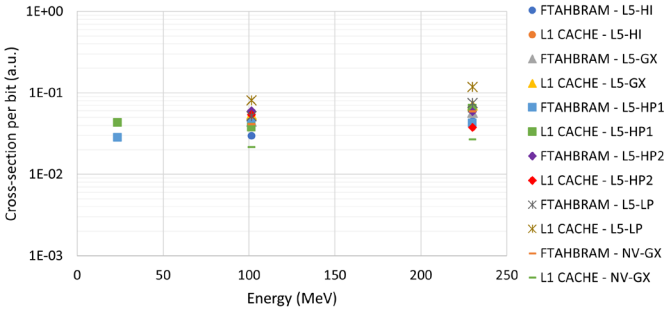

Fig. 3. Total correctable errors cross-section per bit (arbitrary unit) for L1 cache and FTAHBRAM memories of NOEL-V and LEON5 processors at different conditions during proton testing.

VII. GR765 OCTA-CORE PROCESSOR SOC

The GR765 is the Frontgrade Gaisler's next generation of space-grade processor that targets high-performance general-purpose processing with support for mixed-criticality applications [3].

The GR765 will feature an octa-core fault-tolerant architecture that includes the NOEL-V RV64GCV and LEON5 32-bit SPARC V8 processors sharing resources. The user will have the opportunity to select the target architecture as NOEL-V or LEON5, since both processors cannot operate simultaneously. Each processor core is targeted to run at 1 GHz frequency and feature a dedicated FPU and MMU, and a 32 KB L1 cache, connected via multi-port interconnect. Fig. 4 shows the planned GR765 block diagram.

It is expected the GR765 to provide approximately a 20× computational performance improvement compared to the GR740 LEON4 quad-core processor. The GR765 is a product in development and the presented features and characteristics described in this section may change for a future flight model implementation.

The GR765 will be implemented on the STM 28 nm FD-SOI GEO P2 platform. The SEE testing results of the ASIC test chip presented on this work has demonstrated the effectiveness of the fault tolerance features for the NOEL-V and LEON5 cores in the target technology.

VIII. Conclusion

A RISC-V (and LEON5) SoC test chip was built using European STM 28 nm FD-SOI GEO P2 platform. The GR765 space-grade high-performance device, based on NOEL-V and LEON5 processors, is currently in development and will also be implemented on the STM 28 nm FD-SOI. This work has characterized the test chip under heavy ion and proton testing. Results demonstrate the target technology's hardness and the processors' fault tolerance features' effectiveness in handling soft errors.

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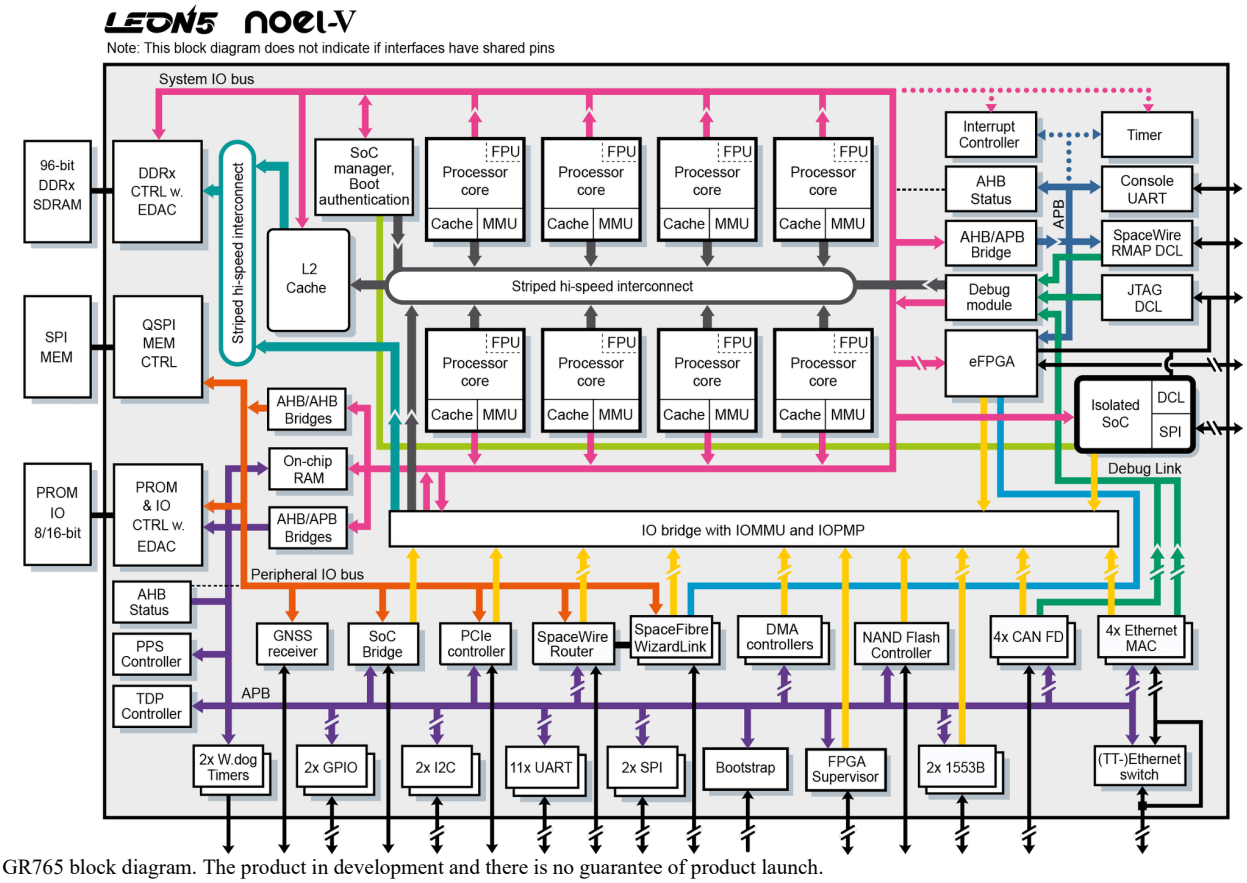

Fig. 4. GR765 block diagram. The product in development and there is no guarantee of product launch.