RISC-V®

GRLIB
SYSTEM-ON-CHIP IP LIBRARY

NOEL-V

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COHERENT ON-CHIP ARCHITECTURE EVALUATION FOR RISC-V MULTI-PROCESSOR

– Ongoing Master Thesis: Cache Coherency Evaluation for Space Applications. Snoop **AMBA AHB** vs. Directory **AMBA CHI**

SUMMARY

With an increasing number of cores in space processors, maintaining coherency with simple protocols is becoming increasingly difficult. Cache coherency protocols ensure the coherency of data over separated caches. With how many cores is it worth it to choose one over the other?

SETUP

- NOEL-V IP Cores
- AHB Bus & CHI NoC
- L1 + L2 Caches + On-Chip RAM
- UVM Simulation Environment

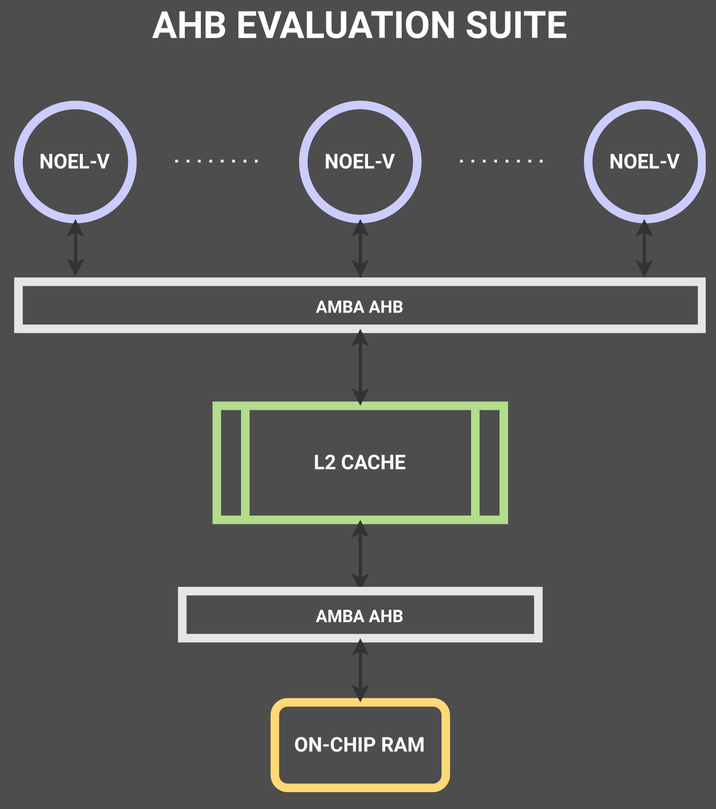
Do you have experience with UVM? We welcome tips on how to utilize its simulation capabilities!

METHOD

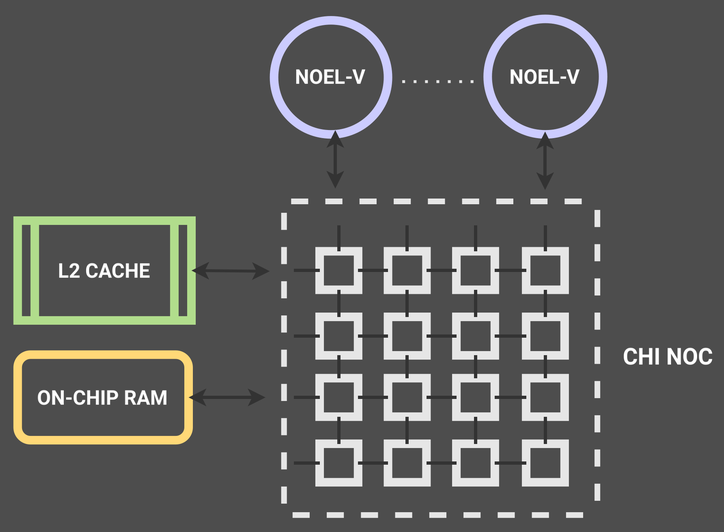
We want to evaluate how much overhead a coherency mechanism protocol carries.

- Is this better done through traffic simulation or a SoC solution?
- How can we represent memory locality through simulation?

AHB EVALUATION SUITE



CHI EVALUATION SUITE



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